2.1A Synchronous Step-Up Converter

FEATURES

- V_{IN} Start Up Voltage: 0.9V
- Output Voltage Range: from 2.5V to 5.5V.
- Up to 94% Efficiency
- Up to 2.1A Continuous Output Current
- Allow EN pin Floating
- Built-in current mode compensation
- Built-in Protection: Over Current, Over Voltage, Over Temperature
- Optional Active High/Low EN pin
- Logic Controlled Shutdown: < 1μA
- Output Disconnect by Shutdown Function
- Built-in Soft Start

APPLICATIONS

- Li-Ion Type Battery Operated Products
- Power Bank
- Handheld Devices
- Portable Products

DESCRIPTION

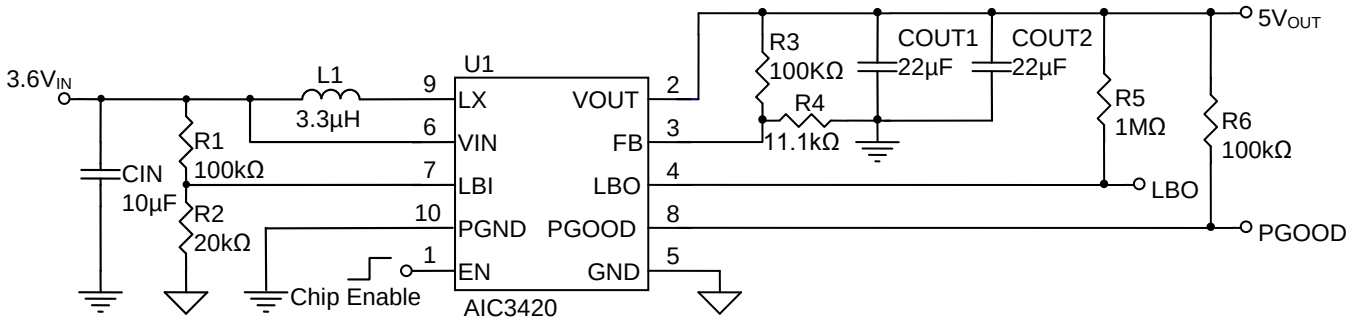
The AIC3420 is a high efficiency, step-up DC/DC converter with high light load efficiency. The true output disconnect function eliminates inrush current and allows Vout to go to zero during shutdown.

The AIC3420 is suited for high current boost application such as battery backup supplies or wireless devices powered by one Li-Ion battery or two Alkaline, Ni-Cd, Ni-MH battery.

The device includes a 50mΩ N-Ch MOSFET switch and a 60mΩ P-Ch MOSFET switch; it can provide high efficiency at 2.1A continuous output current. High efficiency is achieved at light load when PSM Mode operation is entered, where the IC's quiescent current is lower than 20uA on Vout.

The AIC3420 is available in DFN-10 (3x3x0.75-0.5) and SOP-8 Exposed Pad package.

TYPICAL APPLICATION CIRCUITS



Typical Application Circuit for DFN-10 (3x3x0.75-0.5) Package

ORDERING INFORMATION

AIC3420-XXXXXX

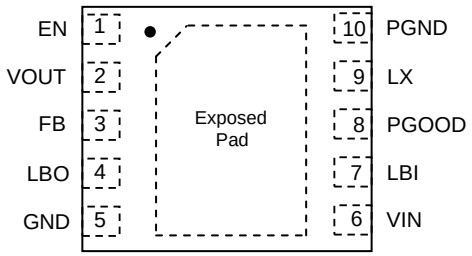
- PACKING TYPE
  TR: TAPE & REEL
  BG: BAG
- PACKAGE TYPE
  DC: DFN-10 (3x3x0.75-0.5)
  R8: SOP-8 Exposed Pad
- G: Green Package
- ENABLE TYPE
  -0: Active Low Enable
  -1: Active High Enable

Example: AIC3420-1GDCTR

→ Active High Enable, in DFN-10 (3x3x0.75-0.5) Package and Tape & Reel Packing Type

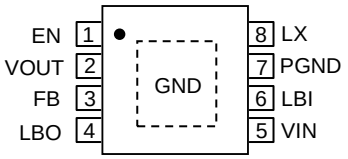
PIN CONFIGURATION

DFN-10 (3x3x0.75-0.5)
TOP VIEW



Note: The exposed pad should be connected with GND pin.

SOP-8 Exposed Pad
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Supply Input Voltage, VIN		-0.3 V to 6V
Output Voltage, VOUT		-0.3 V to 6V
Switch Output Voltage, LX		-0.3 V to 6V
Digital Input Voltage, EN, LBI		-0.3 V to 6V
Digital Output Voltage, LBO, PGOOD		-0.3 V to 6V
Other Pin		-0.3 V to 6V
Operating Ambient Temperature Range T_A		-40°C to 85°C
Operating Maximum Junction Temperature T_J		150°C
Storage Temperature Range T_{STG}		-65°C to 125°C
Lead Temperature (Soldering 10 Sec.)		260°C
Thermal Resistance Junction to Case	SOP-8 Exposed Pad*	15°C/W
Thermal Resistance Junction to Case	DFN-10 (3x3x0.75-0.5)	20°C/W
Thermal Resistance Junction to Ambient	SOP-8 Exposed Pad*	60°C/W
Thermal Resistance Junction to Ambient (Assume no ambient airflow, no heatsink)	DFN-10 (3x3x0.75-0.5)	50°C/W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

*The package is place on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

ELECTRICAL CHARACTERISTICS

(Typical application circuit, T_A=25°C, V_{IN}=3.6V, V_{OUT}=5V, Unless otherwise specified) (Note1)

PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Output Voltage Range	I_{OUT}=0A	V_{OUT}	2.5		5.5	V
Minimum Start Up Voltage	I_{OUT}=0A			0.9		V
Quiescent Current (Non-Switching)		I_{Q0}		20	30	μA
Shut Down Current (Oscillator no switching)	Active High, EN= 0V, V_{IN} =1.1V	I_{SD}		0.3	1	μA
	Active Low, EN= V_{IN}, V_{IN} =1.1V	I_{SD}		0.3	1	μA
Feedback Voltage	I_{OUT}=0	V_{FB}	0.49	0.5	0.51	V
FB Input Leakage Current		I_{FB}		1	50	nA
Maximum Duty Cycle			80	88		%
Minimum Duty Cycle					0	%
NMOS Switch Leakage	V_{SW}=5V			0.1	5	μA
PMOS Switch Leakage	V_{SW}=5V			0.1	10	μA
NMOS Switch On Resistance				50		mΩ
PMOS Switch On Resistance				60		mΩ
EN High Threshold Voltage			1.2			V
EN Low Threshold Voltage					0.25	V
EN Input Current	EN= 5.25V	I_{EN}		10		μA
NMOS Current Limit Setting			4.5	5.5	6.5	A
Power Good threshold voltage	Rising referred to V_{FB}		91	95	99	%
Power Good Hysteresis				5		%
Power Good Delay				10		μS
LBI Voltage Threshold	LBI falling		0.485	0.5	0.515	V
LBI Voltage Hysteresis				10		mV
LBO Output Impedance				150		Ω
Over Temperature Protection				150		°C
Over Temperature Hysteresis				25		°C

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Once the output is started, the IC is not dependant upon the VIN supply.

TYPICAL PERFORMANCE CHARACTERISTICS

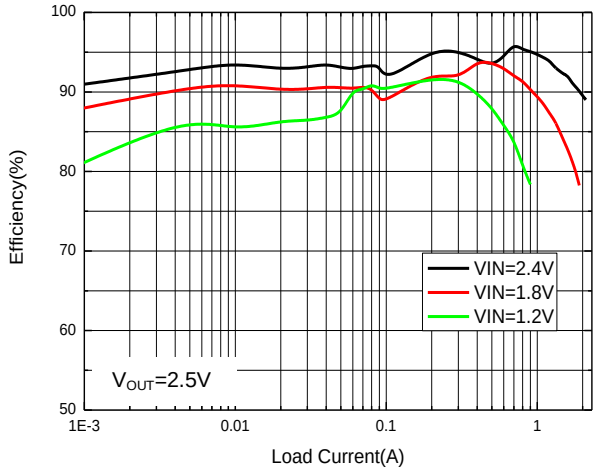


Fig. 1 Efficiency vs. Load Current

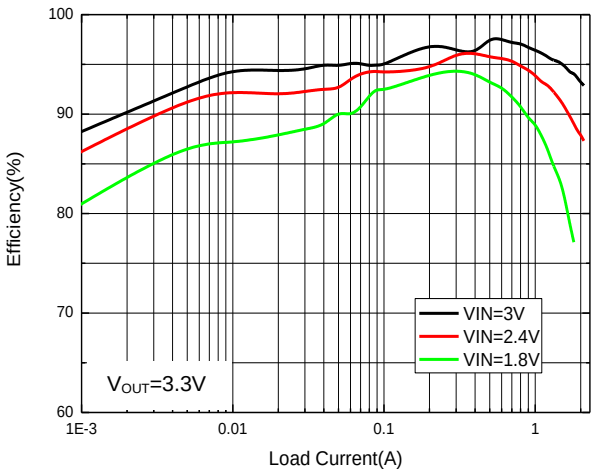


Fig. 2 Efficiency vs. Load Current

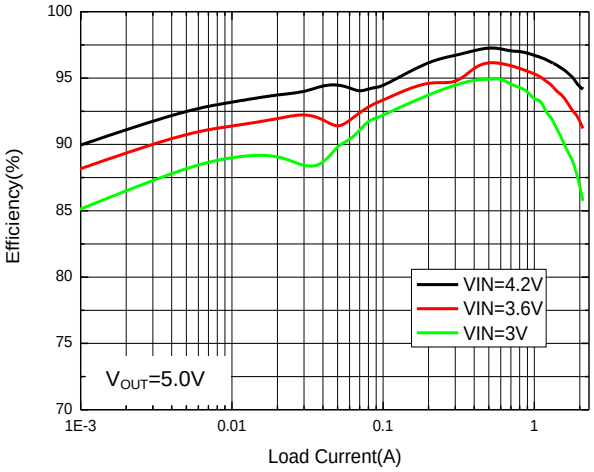


Fig. 3 Efficiency vs. Load Current

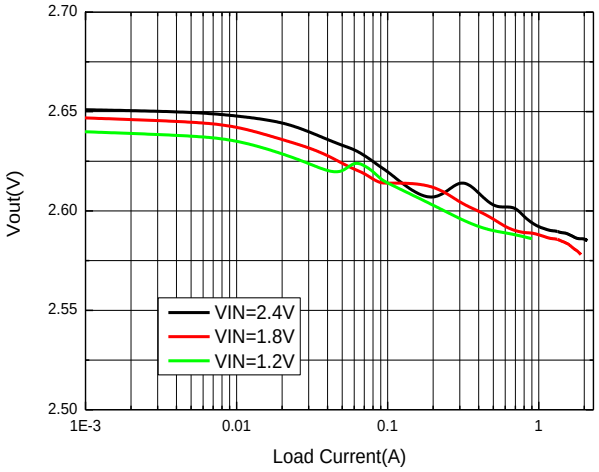


Fig. 4 Output Voltage vs. Load Current

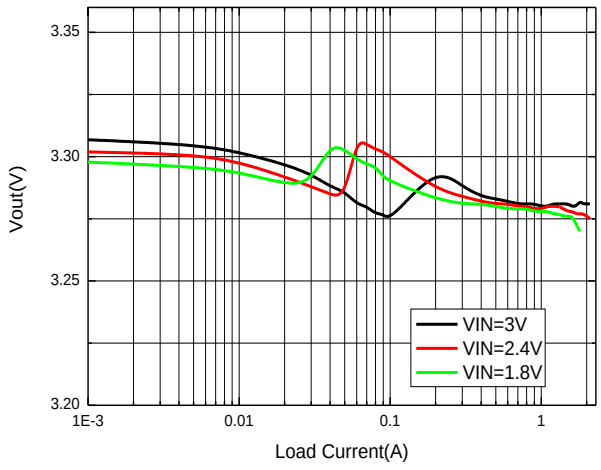


Fig. 5 Output Voltage vs. Load Current

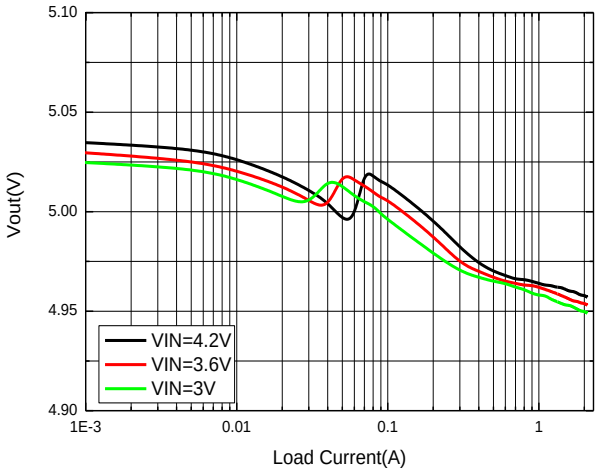


Fig. 6 Output Voltage vs. Load Current

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

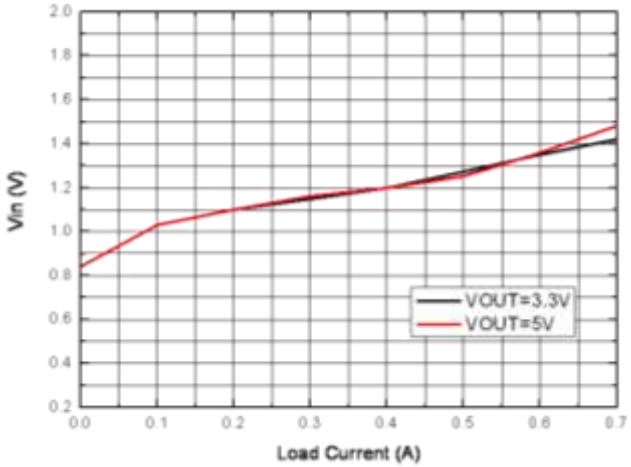


Fig. 7 Start-up Voltage vs. Load Current

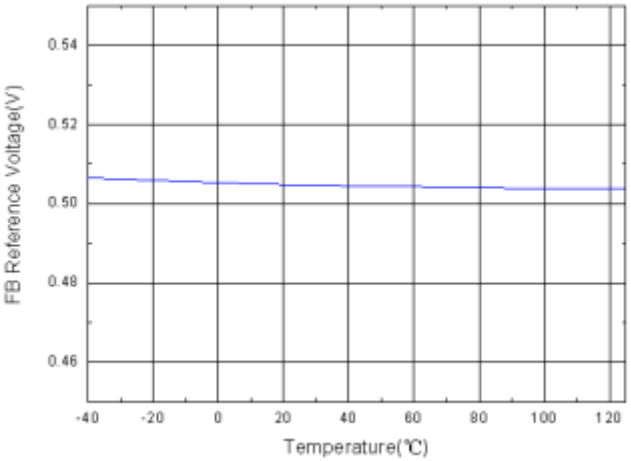


Fig. 8 Reference Voltage vs. Temperature

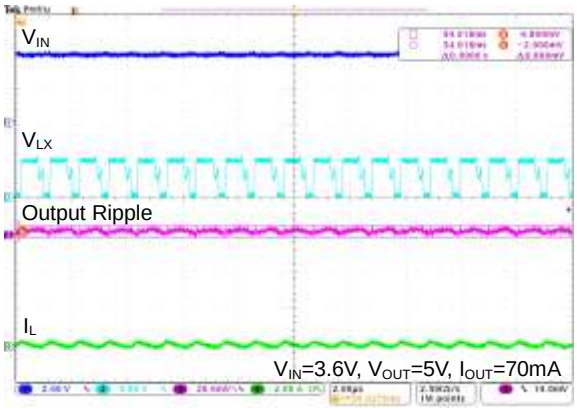


Fig. 9 Switching Waveform at DCM

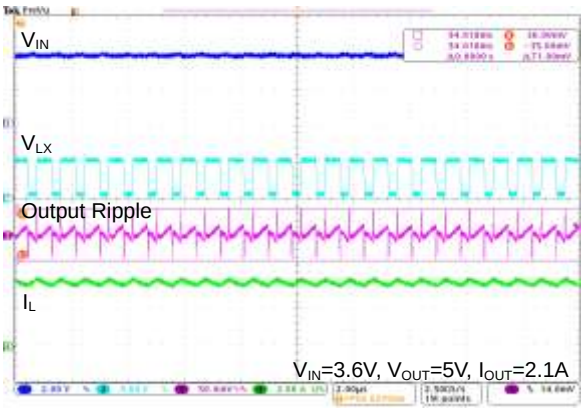


Fig. 10 Switching Waveform at CCM

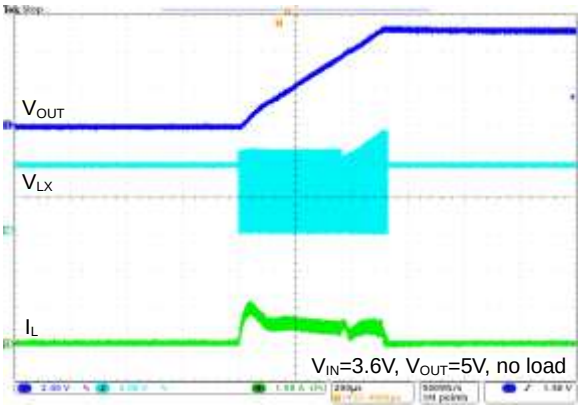


Fig. 11 Start-up Waveform

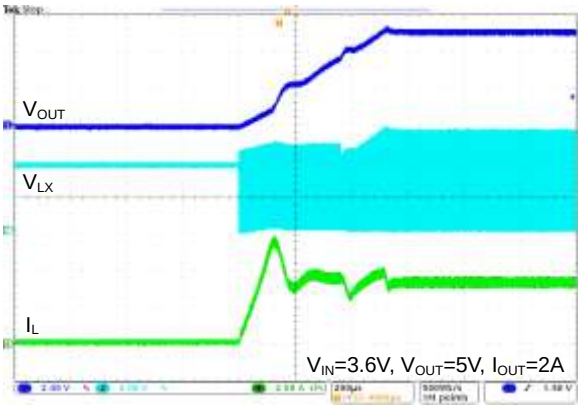


Fig. 12 Start-up Waveform

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

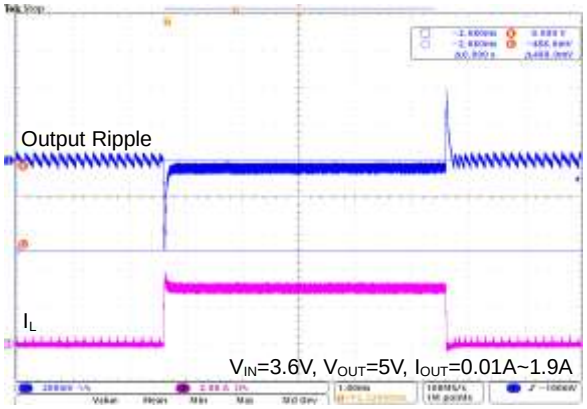


Fig. 13 Load Transient Response

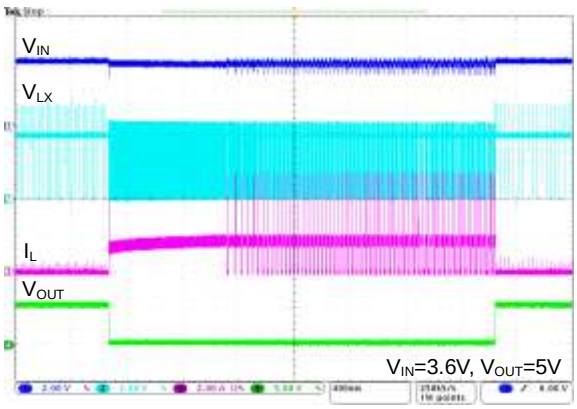


Fig. 14 Short Circuit Waveform

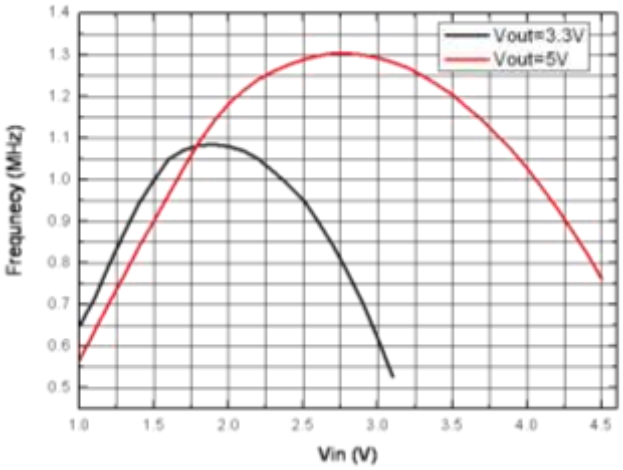
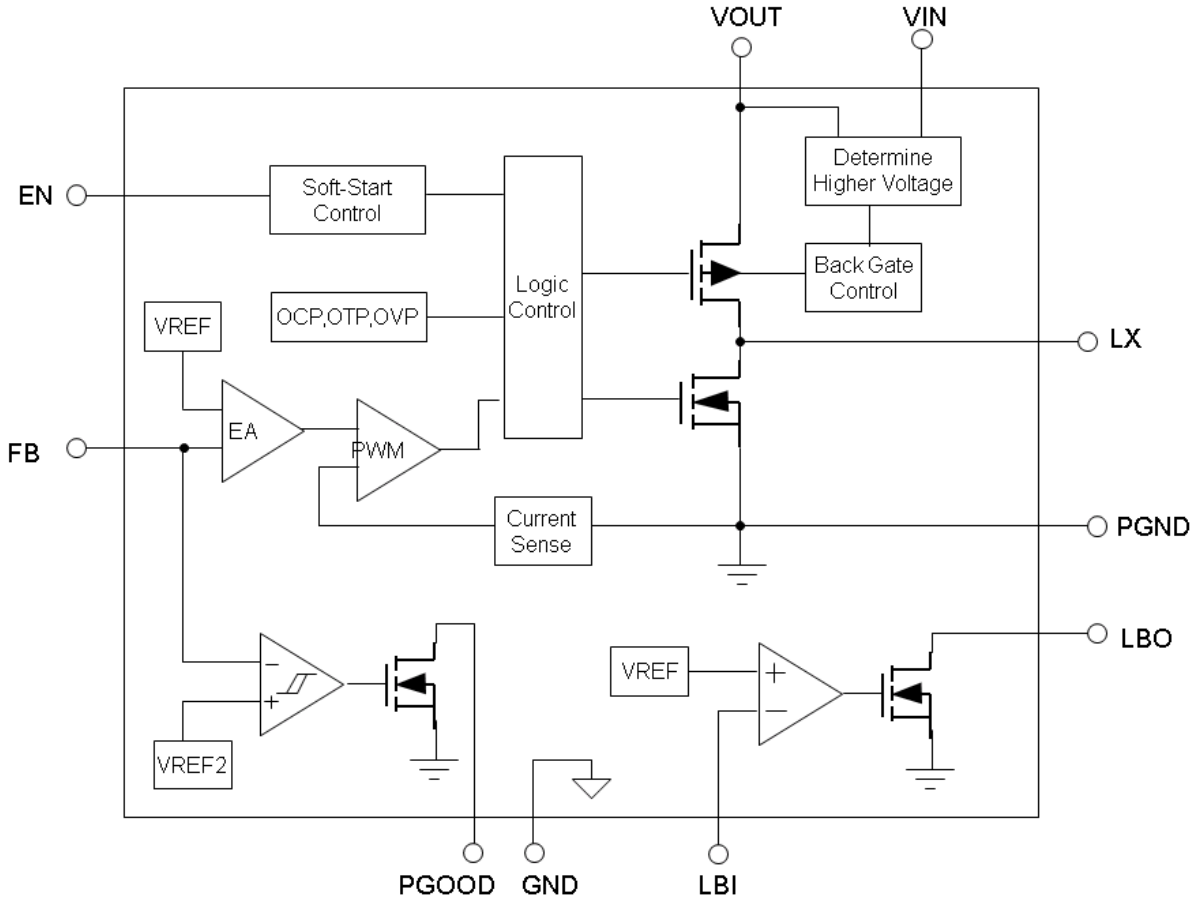


Fig. 15 Switching Frequency vs. Input Voltage

BLOCK DIAGRAM



Functional Block Diagram of AIC3420

PIN DESCRIPTIONS

(For DFN-10 (3x3x0.75-0.5) PACKAGE)

Pin Number	Pin Name	Pin Function
1	EN	Logic Controlled Shutdown Input. There are two versions: Active High Version: EN = High: Normal Operation EN = Low or Floating: IC shutdown Active Low Version: EN = High or Floating: IC shutdown EN = Low: Normal Operation
2	VOUT	Output Voltage Sense and Drain of the Internal Synchronous Rectifier.
3	FB	Feedback Pin. This pin receives the feedback voltage from a resistive divider connect across the output.
4	LBO	Low-Battery Detector Output.
5	GND	Signal Ground.
6	VIN	Input Supply.
7	LBI	Low-Battery Detector Input.
8	PGOOD	Power Good Indicator.
9	LX	Switch Pin. Connect Inductor between VIN and this pin.
10	PGND	Power Ground.

PIN DESCRIPTIONS (Continued)

(For SOP-8 Exposed Pad PACKAGE)

Pin Number	Pin Name	Pin Function
1	EN	Logic Controlled Shutdown Input. There are two versions: Active High Version: EN = High: Normal Operation EN = Low or Floating: IC shutdown Active Low Version: EN = High or Floating: IC shutdown EN = Low: Normal Operation
2	VOUT	Output Voltage Sense and Drain of the Internal Synchronous Rectifier.
3	FB	Feedback Pin. This pin receives the feedback voltage from a resistive divider connect across the output.
4	LBO	Low-Battery Detector Output.
5	VIN	Input Supply.
6	LBI	Low-Battery Detector Input.
7	PGND	Power Ground.
8	LX	Switch Pin. Connect Inductor between VIN and this pin.
9 (Exposed Pad)	GND	Signal Ground.

APPLICATION INFORMATION

The AIC3420 is a synchronous step-up DC-DC converter. It is based on constant Off Time/PSM controller topology. At the beginning of each clock cycle, the main switch (NMOS) is turned on and the inductor current starts to ramp. After the sense current signal equals the error amplifier (EA) output, the main switch is turned off and the synchronous switch (PMOS) is turned on. The device can operate with an input voltage below 2.5V; the typical start-up voltage is 0.9V.

Current Limit Protection

The over current protection can limit the main switch current. The output voltage will be dropped when over current is happened. The over current protection circuit will turn off the main switch once the current exceeds its threshold.

Zero Current Detection

The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier when the inductor current reduces to zero. This prevents the inductor current from reversing in polarity and improves the efficiency at light load condition.

Device Shutdown

For the active high version, when EN is set logic high or floating, the AIC3420 is put into active mode operation. If EN is set logic low, the device is put into shutdown mode and consumes less than 1μA. At the shutdown mode, the synchronous switch will turn off and the output voltage of AIC3420 step-up converter will reduce to 0V. After start-up, the internal circuitry is supplied by VOUT. However, if shutdown mode is enabled, the internal circuitry will be supplied by the input source again.

Low-Battery Detection

AIC3420 contains an on-chip comparator with 10mV internal hysteresis for low battery detection. If the voltage at LBI falls below 0.5V, LBO (an open-drain output) sinks current to GND. The component value of resistor R5 connecting between LBO pin and VOUT pin should be larger than 1MΩ.

Power Good Indicator

AIC3420 contains an on-chip comparator for power good detection. If the output voltage is lower than power good low threshold, PGOOD (an open-drain output) sinks current to GND.

Adjustable Output Voltage

An external resistor divider is used to set the output voltage. The output voltage of the switching regulator (V_{OUT}) is determined by the following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_3}{R_4}\right)$$

Where V_{FB} is 0.5V reference voltage.

Input Inductor Selection

A 1μH~3.3μH input inductor is recommended for most AIC3420 applications. Although small size and high efficiency are major concerns, the inductor should have low core losses at operation frequency and low DCR (copper wire resistance). It is important to ensure the inductor saturation current exceeding the peak inductor current in application to prevent core saturation. For CCM (Continuous Conduction Mode) operation, the peak inductor current can be calculated from:

$$I_{PEAK} = I_{IN(MAX)} + \frac{V_{IN(MIN)} \cdot D_{(MAX)}}{2 \times f_S \cdot L}$$

$$= \frac{I_{OUT(MAX)} \cdot V_{OUT}}{\eta \cdot V_{IN(MIN)}} + \frac{V_{IN(MIN)} \cdot D_{(MAX)}}{2 \times f_S \cdot L}$$

Input Capacitor Selection

Surfaces mount 10μF or greater, X5R or X7R, ceramic capacitor is suggested for the input capacitor. The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AIC3420. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as close as possible to the IC. This keeps the high frequency content of the input current

localized, minimizing EMI and input voltage ripple. Always examine the ceramic capacitor DC voltage coefficient characteristics to get the proper value.

Output Capacitor Selection

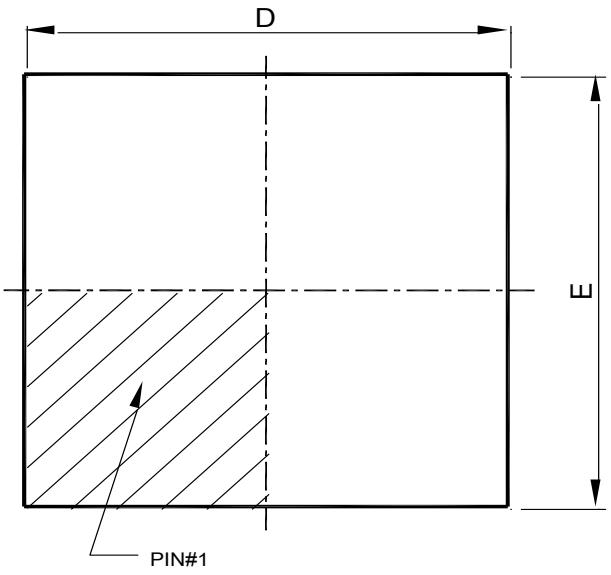
The output capacitor limits the output ripple and provides holdup during large load transitions. Two 22μF, X5R or X7R, ceramic capacitor is suggested for the output capacitor. Typically the recommended capacitor range provides sufficient bulk capacitance to stabilize the output voltage during large load transitions and has the low ESR and ESL characteristics necessary for low output voltage ripple.

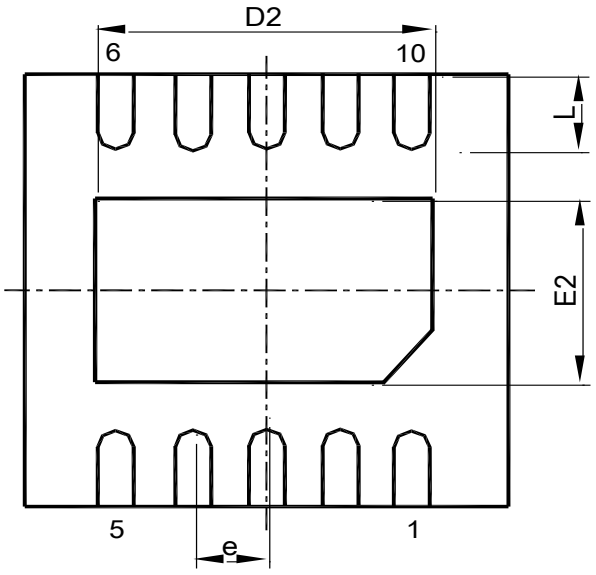
PCB Layout Guidance

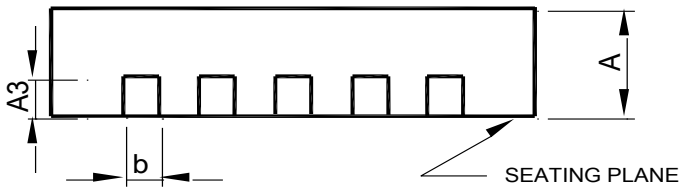
This is a considerably high frequency for DC-DC converters. PCB layout is important to guarantee satisfactory performance. It is recommended to make traces of the power loop, especially where the switching node is involved, as short and wide as possible. First of all, the inductor, input and output capacitor should be as close to the device as possible. Feedback and shutdown circuits should avoid the proximity of large AC signals involving the power inductor and switching node.

PHYSICAL DIMENSION

- **DFN-10 (3x3x0.75-0.5)**





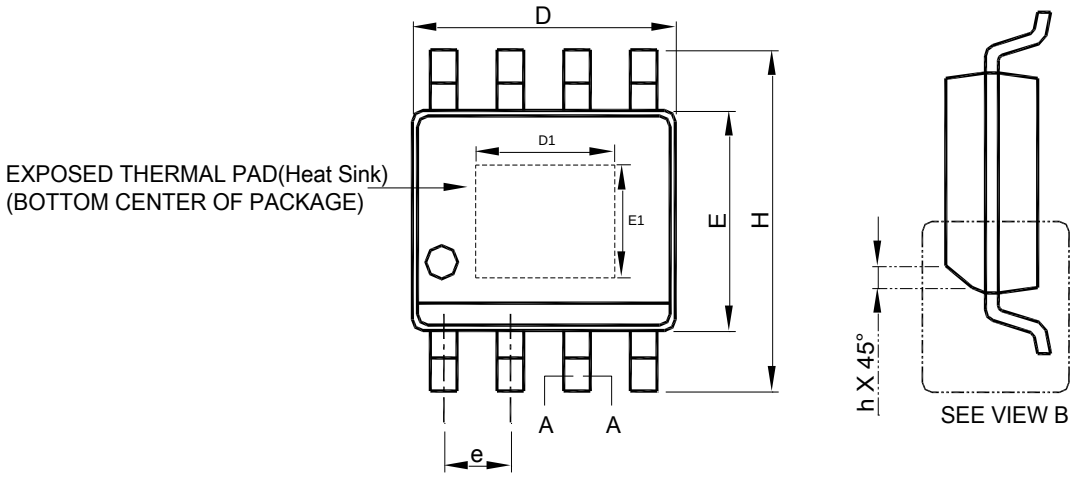


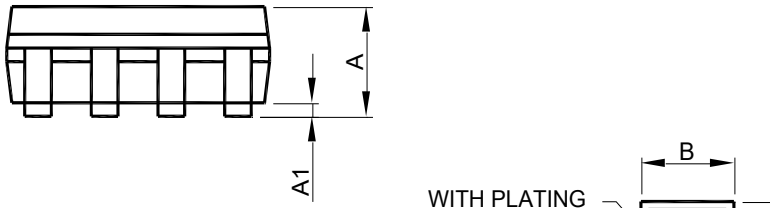
SYMBOL	DFN-10 (3x3x0.75-0.5)	
	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A3	0.20 BSC	
b	0.18	0.30
D	2.90	3.10
D2	2.20	2.70
E	2.90	3.10
E2	1.40	1.80
e	0.5 BSC	
L	0.30	0.50

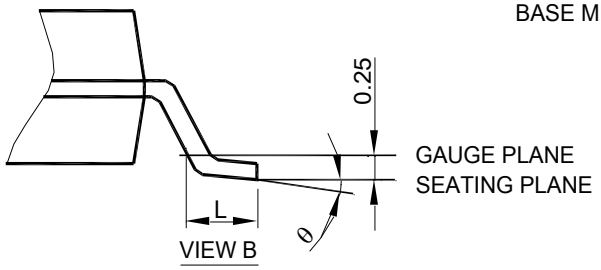
Note : 1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2.CONTROLLING DIMENSIONS : MILLIMETER , CONVERTED INCH
DIMENSION ARE NOT NECESSARILY EXACT.

PHYSICAL DIMENSION (Continued)

- **SOP-8 Exposed Pad**







Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOP-8 Exposed Pad	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
D1	1.50	3.50
E	3.80	4.00
E1	1.0	2.55
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°