4A, 60V, 200kHz Step-Down Converter

FEATURES

- Wide 4.5V to 60V Operating Input Range
- Output Adjustable from 0.8V to 40V
- Standby Current 400μA
- Power Save Mode at Light Load
- Programmable Maximum Peak Current
- 32mΩ Internal Power MOSFET Switch
- 93% Efficiency at V_{IN}=60V, V_{OUT}=12V@2A
- 84.5% Efficiency at V_{IN}=60V, V_{OUT}=5V@2A
- Fixed 200kHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Available in SOP-8 Exposed Pad Package

DESCRIPTION

The AIC2964 is a monolithic step-down switch mode converter. It achieves 4A continuous output current over a wide input supply range with excellent load and line regulation.

The maximum peak current can be programmed by sensing current through an accurate sense resistor.

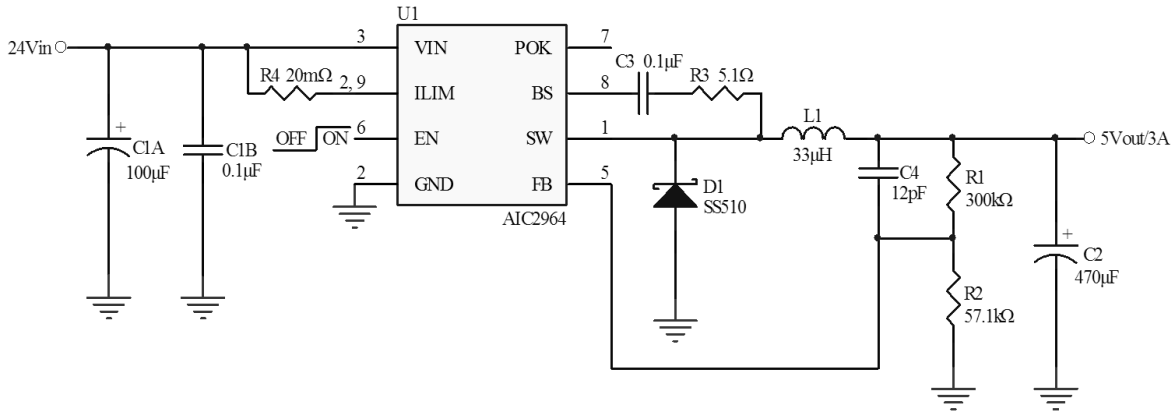
Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The AIC2964 requires a minimum number of readily available standard external components. The AIC2964 is available in SOP-8 exposed pad package.

APPLICATIONS

- Balance Bike
- Ebike
- USB Power Supplies

APPLICATIONS CIRCUIT



Typical Application Circuit

ORDERING INFORMATION

AIC2964XXXXXX

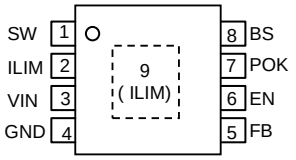
- PACKING TYPE
  TR: TAPE & REEL
  TB: TUBE
- PACKAGE TYPE
  S8E: SOP-8 Exposed Pad
- G: Green Package

Example: AIC2964GS8ETR

→ Green SOP-8 Exposed Pad Package and Tape & Reel Packing Type

PIN CONFIGURATION

SOP-8 Exposed Pad
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

VIN Pin and ILIM Pin Voltage 62V

SW Pin Voltage ..... -0.3V to V_{IN} + 0.3V

BS Pin Voltage ..... V_{SW} + 6.0V

POK Pin Voltage ..... 0V to 45V

All Other Pins Voltage .....-0.3V to +6.5V

Junction Temperature..... 150°C

Lead Temperature ..... 260°C

Storage Temperature Range ..... - 65°C ~ 150°C

Operating Ambient Temperature Range ..... - 40°C ~ 85°C

Thermal Resistance Junction to Case SOP-8 Exposed Pad* ..... 15°C/W

Thermal Resistance Junction to Ambient SOP-8 Exposed Pad* ..... 45°C/W

(Assume no Ambient Airflow)

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

* Measured on approximately 42x45mm^2 of 1 oz copper.

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, T_A=25°C, unless otherwise specified.) (Note1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}		4.5		60	V
Output Voltage	V_{OUT}		0.8		40	V
Feedback Voltage	V_{FB}	$4.5V \leq V_{IN} \leq 60V$	0.785	0.805	0.825	V
Feedback Bias Current	$I_{BIAS(FB)}$	V_{FB} = 0.8V		10		nA
Switch On Resistance	$R_{DS(ON)}$			32		mΩ
Current Limit(Note 2)				(Note 2)		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	160	200	240	kHz
Fold-Back Frequency		V_{FB} = 0V		70		kHz
Boot-Strap Voltage	V_{BST} - V_{SW}			6		V
Minimum On Time(Note 3)	T_{ON}	V_{FB} = 1V		100		ns
Under Voltage Lockout Threshold Rising			3.0	3.3	3.6	V
Under Voltage Lockout Threshold Hysteresis			200			mV
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V		400	700	μA
Thermal Shutdown(Note 3)				160		°C

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Sense resistor defined.

Note 3: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

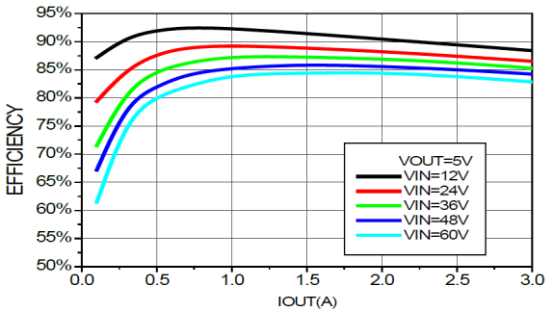


Fig. 1 Efficiency vs. Output Current

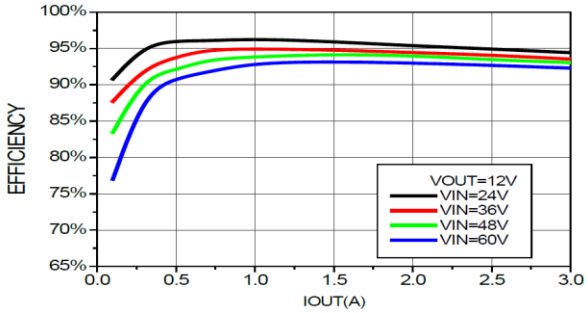


Fig. 2 Efficiency vs. Output Current

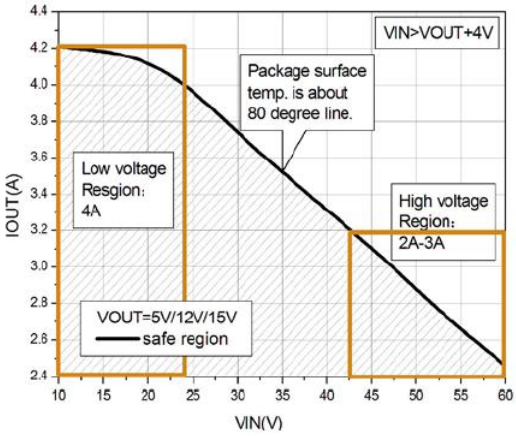


Fig. 3 Maximun Output Current vs. Input Voltage

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Function
1	SW	Switch Output. Connect this pin to the switching end of the inductor.
2, 9	ILIM	Programmable maximum peak current pin by sensing current through an accurate sense resistor between this pin and VIN pin.
3	VIN	Supply Voltage. The AIC2964 operates from a +4.5V to +60V unregulated input. C_{IN} is needed to prevent large voltage spikes from appearing at the input. Put C_{IN} as close to the IC as possible. It is the drain of the internal power device and power supply for the whole chip.
4	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D_1 to C_{IN} ground path to prevent switching current spikes from inducing voltage noise into the part.
5	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency-fold-back comparator lowers the oscillator frequency when the FB voltage is below 250mV.
6	EN	Enable pin. Connect to low off the chip, floating is enable.
7	POK	Power good signal. When FB is less than 90% of 0.8V, PGOOD is low. It is an open-drain output. Use a high value pull-up resistor externally to pull it up to system power supply or its output as next chip enable signal. Connected to GND or floating when don't use this function.
8	BS	Bootstrap. This pin acts as the positive rail for the high-side switch's gate driver. Connect a 100nF ceramic capacitor and 10ohm resistor between this pin and SW.

APPLICATION INFORMATION

Main Control Loop

The AIC2964 is a current mode buck regulator. That is, the error amplifier (EA) output voltage is proportional to the peak inductor current. At the beginning of a cycle, the integrated high side power switch M1 is off; the EA output voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 200kHz clock signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is added to Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and the AIC2964 reverts to its initial M1 off state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop. The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.8V bandgap reference. The polarity is such that a FB pin voltage, which is lower than 0.8V, increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage increases current delivered to the output. An external Schottky Diode (D_1) carries the inductor current when internal power MOS is off.

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R_1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R_1 to be around 300kΩ for optimal transient response. R_2 is then given by:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{0.805} - 1}$$

Table 1 Resistor Selection for Common

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)
3.3	300(1%)	96(1%)
5	300(1%)	57.1(1%)
12	300(1%)	21.4(1%)
15	300(1%)	16.9(1%)
24	300(1%)	10.2(1%)
32	300(1%)	7.6(1%)

Selecting the Inductor

33µH to 100µH inductor with a DC current rating of at least 30% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 50mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{SW}}$$

Where ΔI_L is the inductor ripple current. Choose inductor current ripple to be approximately 30%~40% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and also the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current from pass to the input. For most

applications, a 47µF to 100µF electrolytic capacitor is sufficient.

Selecting the Output Capacitor

The output capacitor keeps output voltage ripple small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. A 220µF to 470µF electrolytic capacitor is recommended.

ILIM sense resistor

Power current flows into the chip via the external accuracy sense resistor which defined the maximum peak current. In guarantee under the normal start up with full load, the sense resistor is recommended use the larger value to ensure less surge current and output short power dissipation. The sense resistor value should be reduced when used it at low temperature situation to ensure enough startup energy.

Table 2 Sense Resistor Selection

Max. output current （A）	R_{sense}（mΩ）
2	30
3	20
4	15

Loop compensation

A 3.3pF to 22pF ceramic capacitor connected between FB and OUT can optimize the loop stability for both bandwidth and phase margin, recommended a 4.7pF to12pF ceramic capacitor in most case.

POK

Power good signal. POK is an open-drain output, can be used as enable signal for next level chip. When FB is less than 90% of 0.8V, PGOOD is low, when output is ready, by connected external pull-up resistor become high to turn on next level chip.

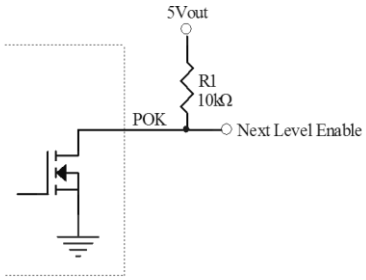


Fig. 4 Power Good Circuit

PCB Layout

(1) Under the large output current and high input voltage case, the schottky diode and the converter is the main heat source, don't put them too close, the PCB layout should keep enough area for heat dissipation. Recommended ratio is 6:4 for schottky diode and the converter, for the cost issues, the normal selection of PCB is 1oz thickness, the thick solder tin is benefit on heat dissipation.

(2) ILIM is internal connected the power MOS, the heat dissipation should be considered for this pin.

(3) The large current path (ILIM, SW) should be put closer the converter as possible, use short, straight, wide copper foil connect.

(4) Input capacitor should be put as close as possible to VIN pin and GND.

(5) The loop of input capacitor, internal power MOS and schottky diode is the highest di/dt radiation region, reduce this region as possible. A 0.1µF ceramic capacitor can be used to form a small loop with internal power MOS and schottky diode, which can reduce the switch ringing caused by PCB parasitic inductor.

(6) The outside feedback resistor should be placed nearby the FB pin and keep away from SW node.

Figures 5 to 7 show the layout diagrams of AIC2964.

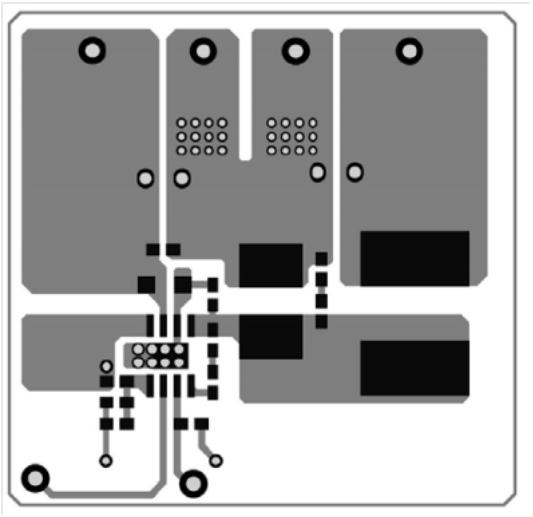


Fig. 5 Top Layer

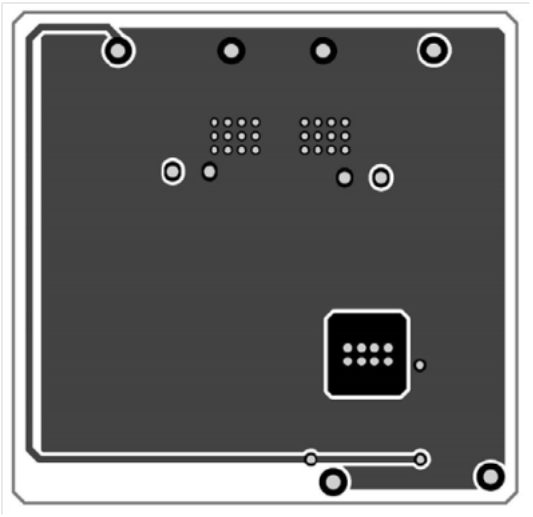


Fig. 6 Bottom Layer

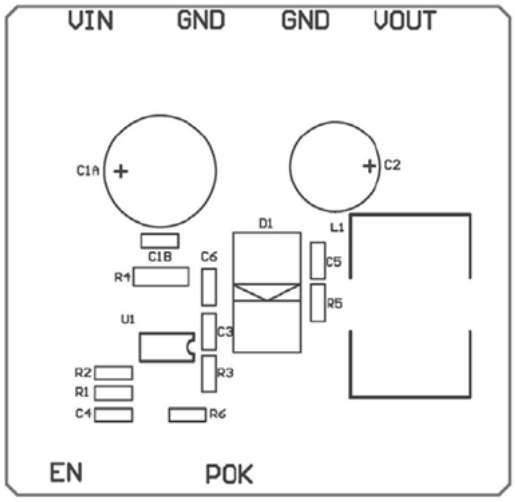


Fig. 7 Top Component Placement

APPLICATION EXAMPLES

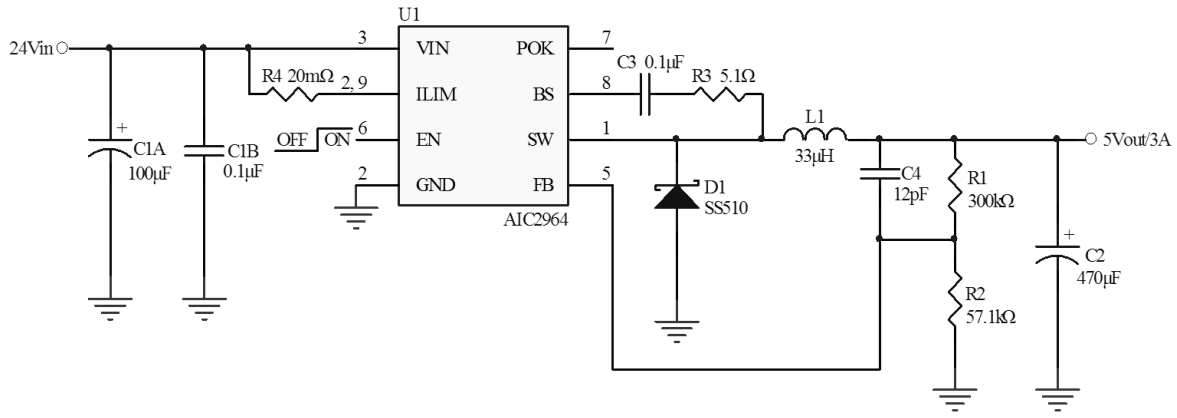


Fig. 8 AIC2964 Application Circuit for 5V/3A Output Application

Table 3 BOM List for 5V/2A Output Application

Ref	Value	Description	Package	Manufacturer	Qty	Manufacturer P/N
C1A	100µF	Electrolytic,100V	ELC SMD	jiang hai	1	VTD-100V100
C1B	0.1µF	Ceramic capacitor,100V	0603	muRata	1	GRM188R72A104K
C2	470µF	Electrolytic,16V	ELC SMD	jiang hai	1	VTD-16V470
C3	100nF	Ceramic capacitor, 100V, X7R	0603	muRata	1	GRM188R72A104K
C4	12pF	Ceramic, capacitor 50V, X7R	0603	muRata	1	GRM188R71H120K
D1	5A	Schottky Diode, SS510, 100V, 5A	SMC		1	SS510
L1	33µH	Inductor CDRH127, 3A, 58mΩ	CDRH127		1	
R1	300kΩ	Film Res., 1%	0603	Panasonic	1	ERJ-3EKF3003V
R2	57.1kΩ	Film Res., 1%	0603	Panasonic	1	ERJ-3EKF5712V
R3	5.1Ω	Film Res., 1%	0603	Panasonic	1	
R4	30mΩ	Film Res., 1%	1206		1	
U1		DC-DC convertor	SOP-8E	AIC2964	1	

Note: recommended to use a low V_F schottky diode for efficiency promotion.

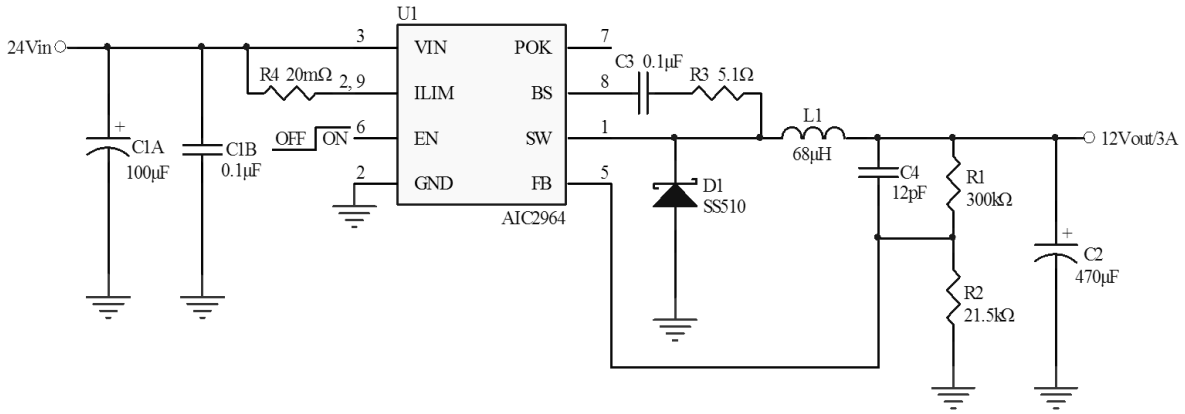


Fig. 9 AIC2964 Application Circuit for 12V/3A Output Application

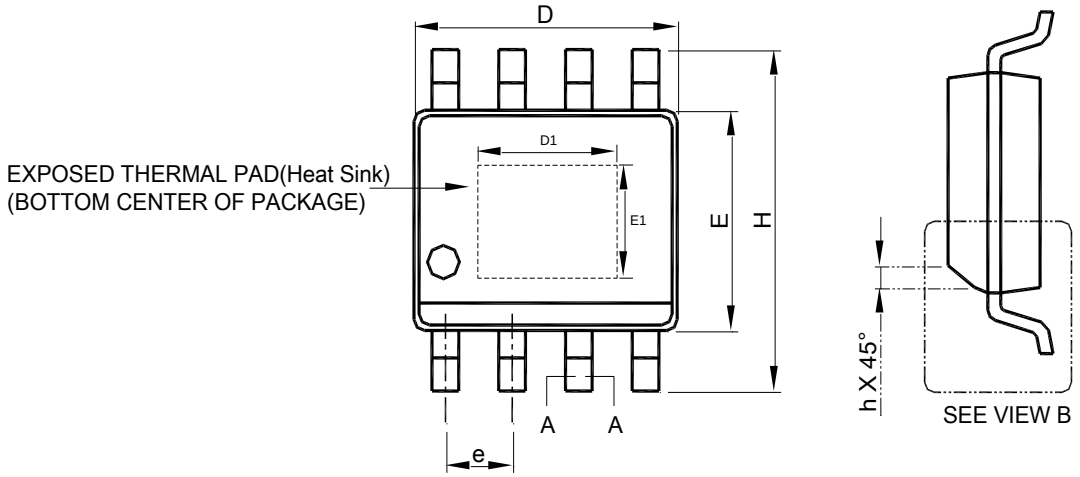
Table 4 BOM List for 12V/2A Output Application

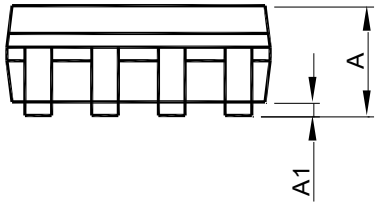
Ref	Value	Description	Package	Manufacturer	Qty	Manufacturer P/N
C1A	100μF	Electrolytic,100V	ELC SMD	jiang hai	1	VTD-100V100
C1B	0.1μF	Ceramic capacitor,100V	0603	muRata	1	GRM188R72A104K
C2	470μF	Electrolytic,25V	ELC SMD	jiang hai	1	VTD-25V470
C3	100nF	Ceramic capacitor, 100V, X7R	0603	muRata	1	GRM188R72A104K
C4	12pF	Ceramic, capacitor 50V, X7R	0603	muRata	1	GRM188R71H120K
D1	5A	Schottky Diode, SS510, 100V, 5A	SMC		1	SS510
L1	68μH	Sendust core, 4A	50125		1	
R1	300kΩ	Film Res., 1%	0603	Panasonic	1	ERJ-3EKF3003V
R2	21.5kΩ	Film Res., 1%	0603	Panasonic	1	ERJ-3EKF2152V
R3	5.1Ω	Film Res., 1%	0603	Panasonic	1	
R4	20mΩ	Film Res., 1%	1206		1	
U1		DC-DC convertor	SOP-8E	AIC2964	1	

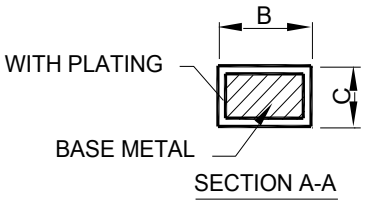
Note: recommended to use a low V_F schottky diode for efficiency promotion.

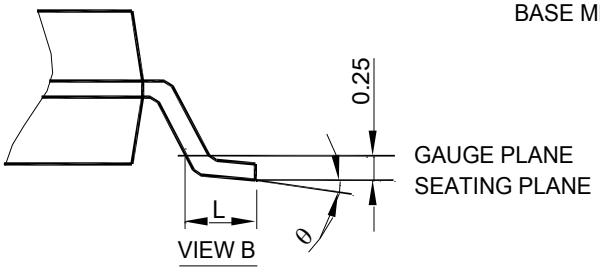
PHYSICAL DIMENSIONS

- **SOP-8 Exposed Pad**









Note : 1. Refer to JEDEC MS-012E.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOP-8 Exposed Pad	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
D1	1.50	3.50
E	3.80	4.00
E1	1.0	2.55
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°