AIC1533

Triple-Output LCD Power Supply

FEATURES

- One Low Dropout Linear Regulator
  Dropout Voltage 500mV at 0.3A Output Current
- Dual Adjustable Charge Pump
  Up to +30V Positive Output
  Down to -10V Negative Output
- Power Up Sequencing and Adjustable Delay time
- Power-Saving Shutdown Mode (0.1μA typical)
- Operating Supply Voltage: 12V
- 1MHz Operation Frequency
- Internal Current Limit and Thermal Protection built in LDO part
- Few External Components Required

APPLICATIONS

- LCD Monitor Panel Module
- LCD TV Panel Module

DESCRIPTION

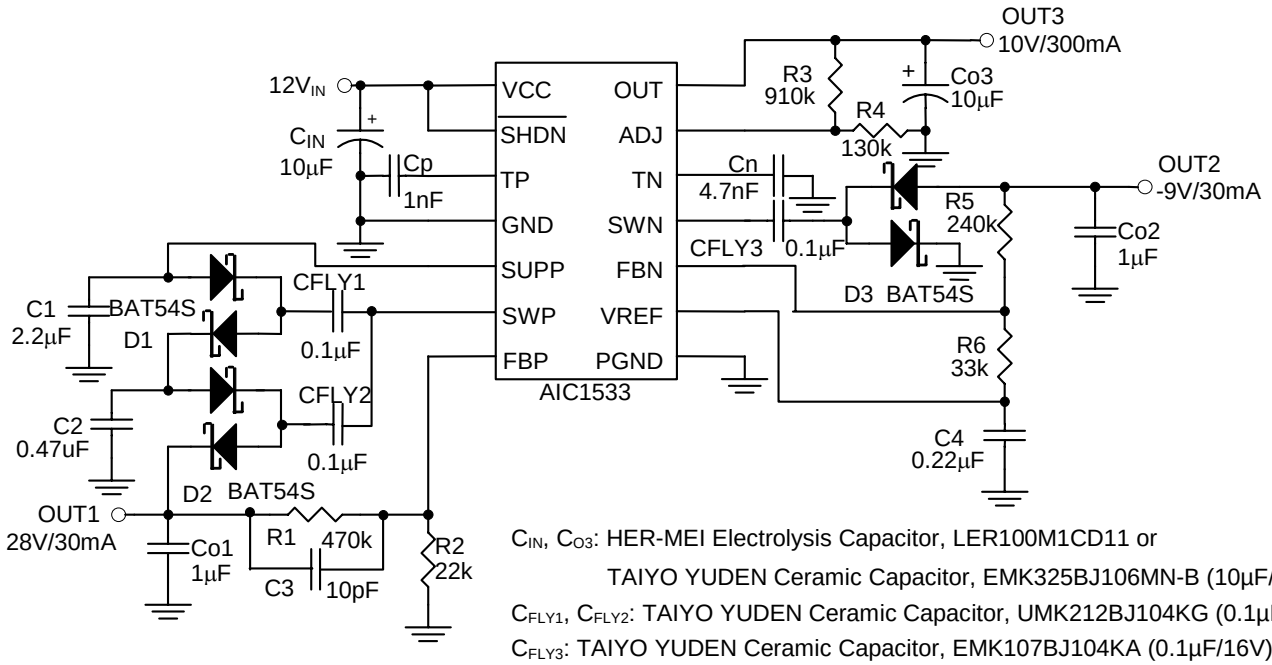
AIC1533, composed of dual charge pumps and a regulator, provide three independent regulated voltages designed for using in thin-film transistor (TFT) liquid crystal display (LCD).

The main regulator has an adjustable output voltage and a low dropout voltage of 500mV at 300mA load current is performed.

The dual charge pumps independently regulate a positive output and a negative output. AIC1533 has thermal shutdown capability and survives a continuous short circuit from output to ground. A unique control scheme minimizes output ripple as well as output capacitance for both charge pump.

1MHz-switching frequency of AIC1533 provides a low noise, low cost total solution. The device operates up to 15V supply voltage and is available in 14-lead SOP and 16-lead TSSOP package.

TYPICAL APPLICATION CIRCUIT



C$_{IN}$, C$_{O3}$: HER-MEI Electrolysis Capacitor, LER100M1CD11 or
TAIYO YUDEN Ceramic Capacitor, EMK325BJ106MN-B (10µF/16V)
C$_{FLY1}$, C$_{FLY2}$: TAIYO YUDEN Ceramic Capacitor, UMK212BJ104KG (0.1µF/50V)
C$_{FLY3}$: TAIYO YUDEN Ceramic Capacitor, EMK107BJ104KA (0.1µF/16V)
C$_{O1}$: TAIYO YUDEN Ceramic Capacitor, UMK212F105ZG (1µF/50V)
C$_{O2}$: TAIYO YUDEN Ceramic Capacitor, EMK212F105KG (1µF/16V)
D$_1$~D$_3$: WTE Schottky Diode, BAT54S

Fig.1 TFT-LCD Power Application

ORDERING INFORMATION

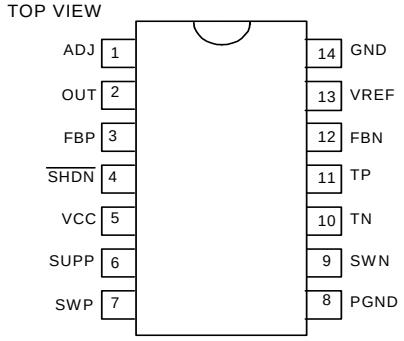
AIC1533XXXX

- PACKING TYPE
  TB: TUBE
  TR: TAPING & REEL
- PACKAGING TYPE
  S: SOP-14
  L: TSSOP-16
- C: COMMERCIAL
  P: LEAD FREE COMMERCIAL
  G: GREEN PACKAGE

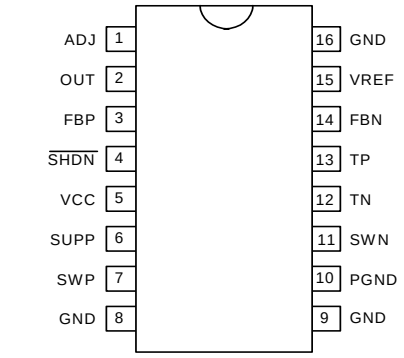
Example: AIC1533CLTR
→ in TSSOP-16 Package & Taping & Reel Packing Type
AIC1533PSTR
→ in Lead Free SOP-14 Package & Taping & Reel Packing Type

PIN CONFIGURATION

SOP-14
TOP VIEW



TSSOP-16
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

VCC, $\overline{SHDN}$ to GND ..... -0.3V to 18V
FBN, FBP, VREF, ADJ, TN, TP ..... -0.3V to 8V
SWN, SWP ..... -0.3V to (Vcc+0.3V)
PGND to GND ..... ±0.3V
Operating Temperature ..... -40°C to 85°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance Junction to Ambient SOP-14 ..... 100°C/W
(Assume no ambient airflow, no heatsink) TSSOP-16 ..... 120°C/W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TEST CIRCUIT

Refer to TYPICAL APPLICATION CIRCUIT.

ELECTRICAL CHARACTERISTICS

(V_{IN}=12V, C_{O1}=C_{O2}=1μF, C_{O3}=10μF, C_{FLY1}=C_{FLY2}=C_{FLY3}=0.1μF, T_A=25°C, unless otherwise specified.)
(Note 1)

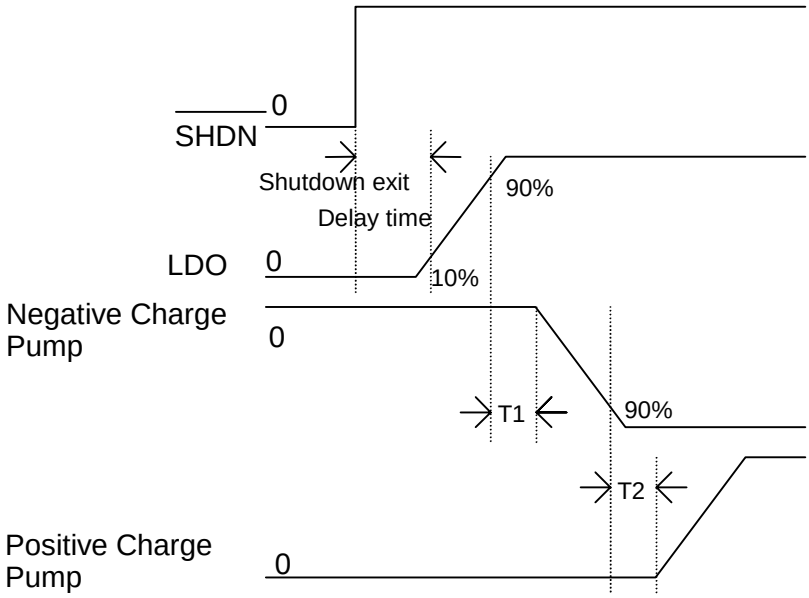
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage Range		10	12	15	V
Quiescent Current	$V_{\overline{SHDN}}$=2.4V, I_{OUT}= 0mA	0.6	1.2	2.0	mA
Standby Current	$V_{\overline{SHDN}}$=0.6V,Output OFF			1	μA
Thermal Shutdown Temperature			155		°C
LOW DROPOUT LINEAR REGULATOR TERMINAL SPECIFICATION					
Adjustable Voltage		1.225	1.25	1.275	V
Line Regulation	V_{IN} =12~15V, V_{OUT3}=10V, I_{OUT3}=1mA			1	%
Load Regulation	V_{IN} =12V, I_{OUT3}=0.1~300mA			1	%
Continuous Output Current	V_{IN} =12V		300		mA
Current Limit	V_{IN} =12V, V_{OUT3}=0V (Note2)	350		700	mA
Dropout Voltage	I_{OUT3}=300mA			500	mV

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP TERMINAL SPECIFICATION					
FBP Threshold		1.225	1.25	1.275	V
FBN Threshold		-30	0	30	mV
VREF Voltage	I_{REF}=250μA	1.231	1.25	1.269	V
Continuous Output Current	V_{IN} =12V			30	mA
TP/TN Bias Current		3	5	7	μA
TP/TN Input Threshold		1.225	1.25	1.275	V
Switching Frequency		0.70	1	1.30	MHz
Internal Switch On-Resistance	SUPP switch		5	10	Ω
	SWP switch		5	10	
	SWN switch		5	10	
SHUTDOWN TERMINAL SPECIFICATIONS					
$\overline{SHDN}$ Pin Current	$V_{\overline{SHDN}}$=2.4V		0.1	1	μA
$\overline{SHDN}$ Pin Voltage	Output ON	2.4			V
	Output OFF			0.6	

Note 1: Specifications are production tested at T_A=25°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 2: Current limit is measured by pulse testing.



T1 set by C_N

T2 set by C_P

Fig. 2 Power Up Sequencing

TYPICAL PERFORMANCE CHARACTERISTICS

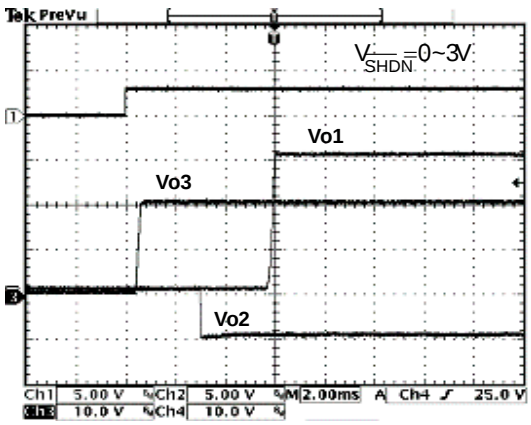


Fig. 3 Power- Up Sequence

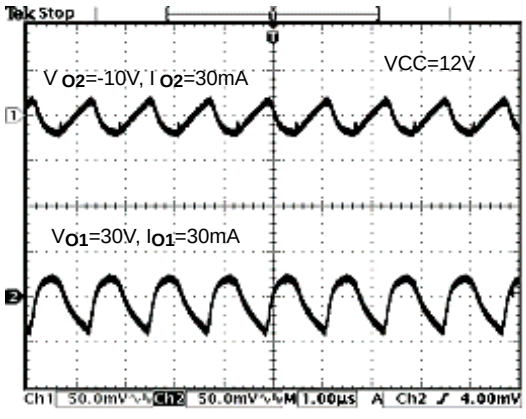


Fig 4. Ripple Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

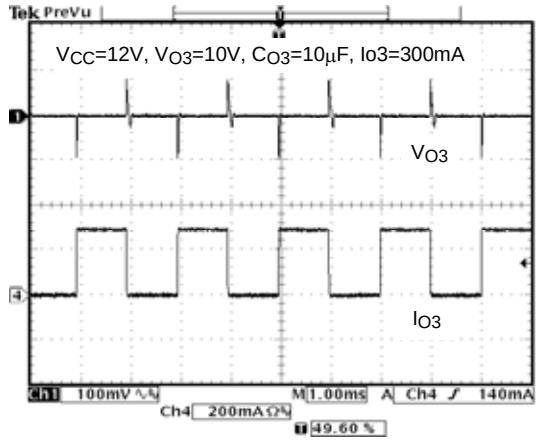


Fig. 5 LDO Load Transient Response

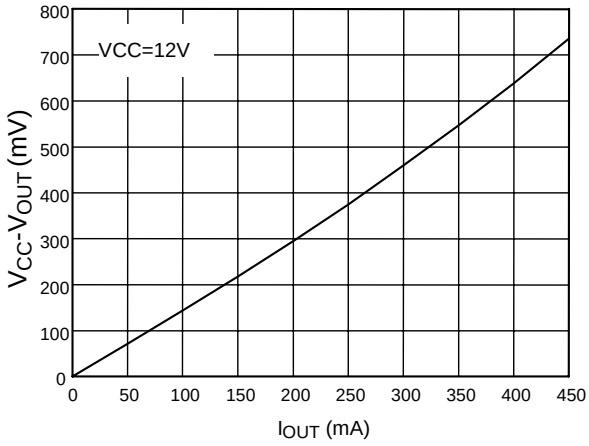


Fig. 6 Dropout Voltage vs. LDO Load

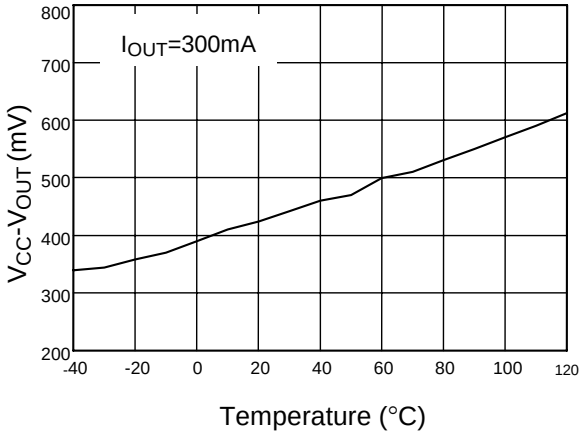


Fig. 7 LDO Dropout Voltage vs. Temperature

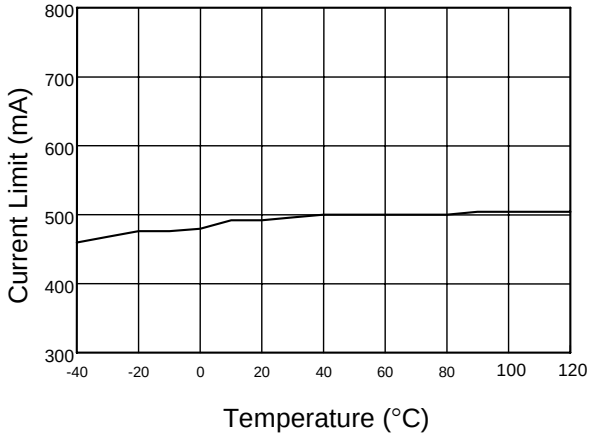


Fig. 8 LDO Current Limit vs. Temperature

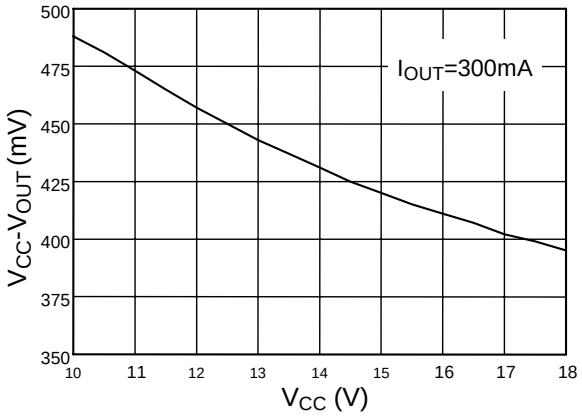


Fig. 9 LDO Dropout Voltage vs. Input Voltage

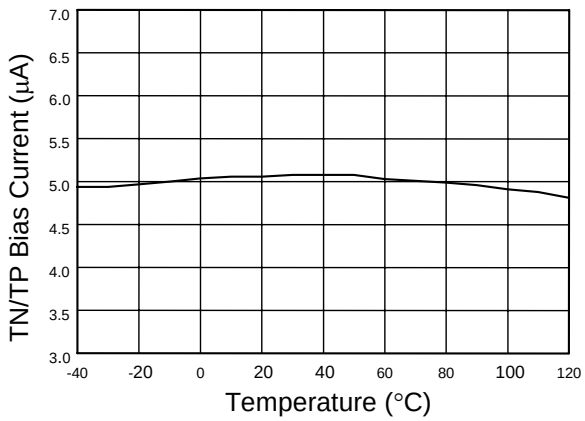


Fig. 10 TN/TP Bias Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

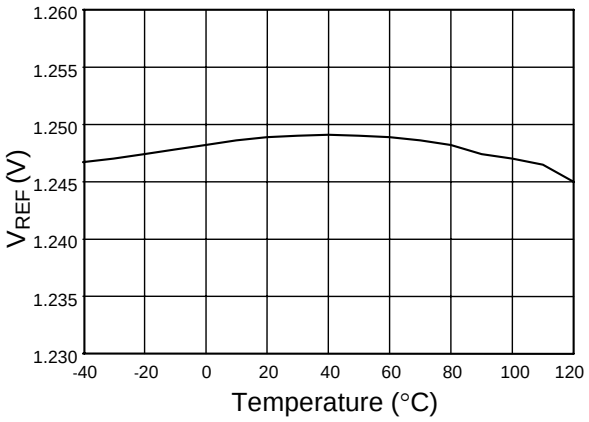


Fig. 11 V_{REF} vs. Temperature

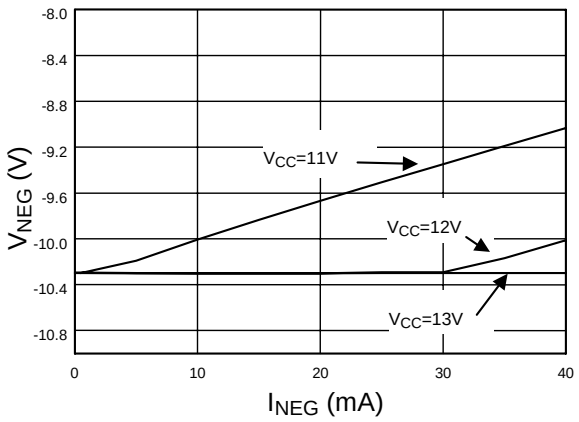


Fig. 12 Negative Charge-Pump vs. Load Current

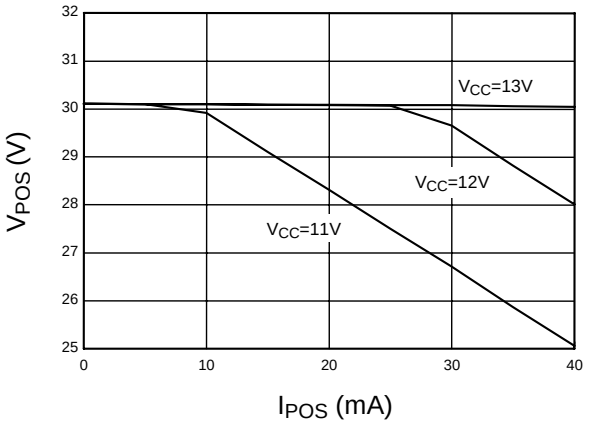


Fig. 13 Positive Charge Pump vs. Load Current

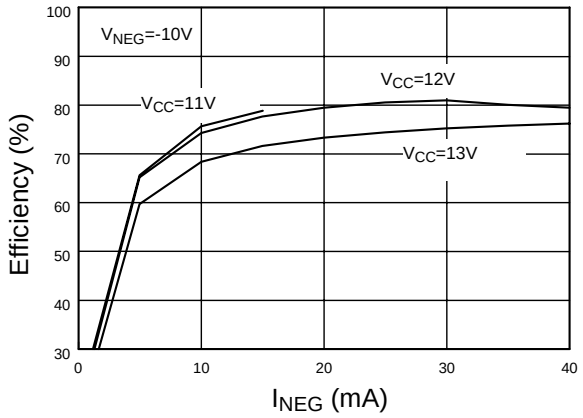


Fig. 14 Negative Charge-Pump vs. Load Current

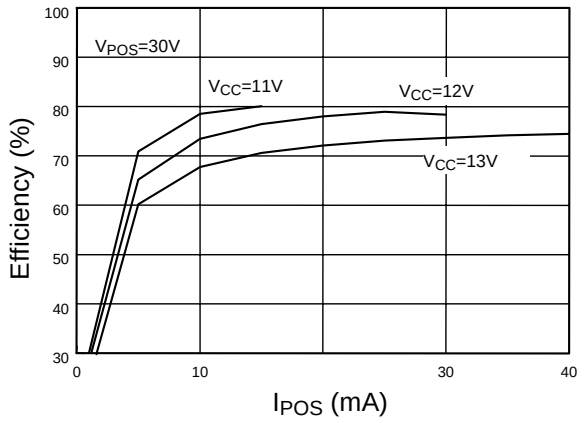
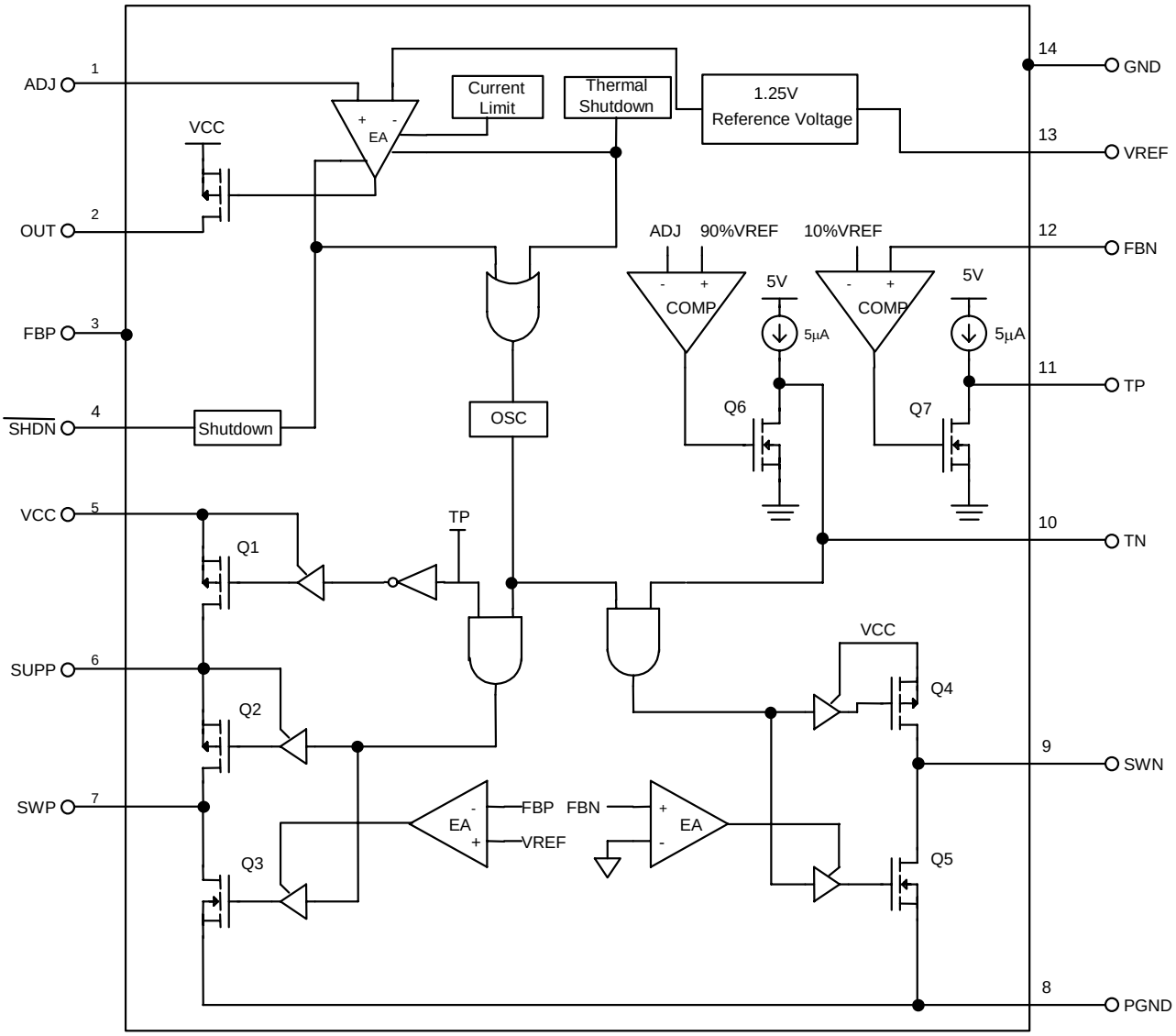


Fig. 15 Positive Charge-Pump Efficiency vs. Load Current

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN 1: ADJ - Providing V_{ADJ}=1.25V (typ.) for adjustable V_{OUT}.

PIN 2: OUT - Adjustable LDO regulator output.

PIN 3: FBP - Positive charge pump feedback input. Regulates to 1.25V typical.

PIN 4: $\overline{SHDN}$ - Active-Low logic level shutdown input. Connecting $\overline{SHDN}$ to VCC for typical operation.

PIN 5: VCC - Supply input.

PIN 6: SUPP - Positive charge pump supply pin. It monitors negative charge pump.

PIN 7: SWP - Positive charge pump driver output. Output high level is VCC, and low level is GND.

PIN 8: PGND - Power ground. Connecting to GND.

PIN 9: SWN - Negative charge pump driver output. Output high level is VCC, and low level is GND.

PIN 10: TN - Programmable delay time pin. The capacitor on this pin sets negative charge pump to provide independent time control. Or TN connects to high level directly if it is not in use for programming delay time.

PIN 11: TP - Programmable delay time pin. The capacitor on this pin sets positive charge pump to provide independent time control. Or TP connects to high level directly if it is not in use for programming delay time.

PIN 12: FBN - Negative charge pump feedback input. Regulates to 0V typical.

PIN 13: VREF - Internal reference bypass terminal. Connecting a 0.22μF capacitor to ground. Providing a positive voltage greater than negative feedback voltage to obtain a positive voltage for FBN.

PIN 14: GND - Ground. Tie GND pin directly to local ground plane to obtain best performance.

APPLICATION INFORMATION

Introduction

AIC1533 is composed of dual charge pumps and a regulator to provide three independent regulated voltages exclusively designed for thin-film transistor (TFT) liquid crystal display (LCD) applications. LDO regulator has an adjustable output voltage with a low dropout voltage of 500mV at 300mA load current. Two independent charge pumps regulate a positive output and a negative output by using a 1MHz switching frequency, and a pulse-width-modulation (PWM) architecture.

AIC1533 provides a start-up sequence function with an adjustable start-up delay time. In shutdown mode, it only consumes 0.1μA supply current. AIC1533 also features an internal current limit and thermal shutdown protection.

Operation

As Fig. 16 shows, two internal MOSFETs - Q2, Q3, and external components comprise a positive charge pump, whose output is three times as much as input voltage. After delay time, which determined by C_P, Q1 turns on. During on state, which indicates Q2 is at off stage and Q3 at on stage, C_{FLY1} connects V_{CC} and PGND and is charged by V_{CC}.

During off state, Q2 at on stage and Q3 off stage, voltage of C2 is the addition of V_{CC} and V_{CFLY1}. And then go back to on state with voltage of C_{FLY2} equal to $V_{C2,}$ which is twice as much voltage as V_{CC}. Lastly, the system goes to off state, voltage of Co1 is the addition of V_{CC} and C_{FLY2}, that is, three times as much voltage as V_{CC}.

Fig.17 shows the structure of a negative charge pump. During on state, which represents Q4 at on stage and Q5 at off stage, voltage of C_{FLY3} is equal to V_{CC}. During off state, indicating Q4 at off stage and Q5 on stage, SWN pin connects to PGND directly, and voltage of Co2 equals to $-V_{CC}$.

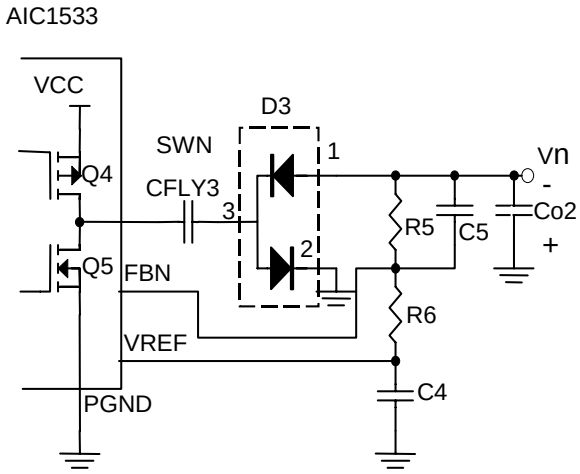


Fig. 17 Structure of Negative Charge Pump

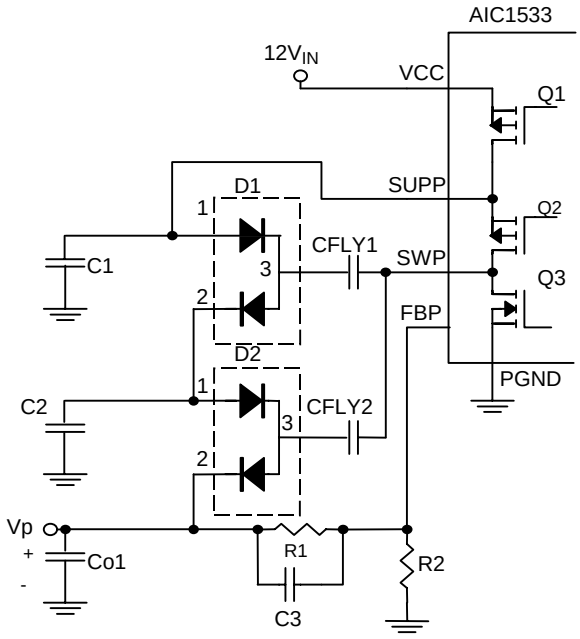


Fig.16 Structure of Positive Charge Pump

Power-Up Sequence And Adjustable Delay Time

For thin-film transistor (TFT) liquid crystal display applications, power-up sequence of three output voltages is required. Fig. 3 indicates the power-up sequence of AIC1533. After shutdown exit delay time, output of LDO starts rising. When it reaches to 90% of normal voltage, which is determined by an external resistor divider, C_N starts being charged from 5μA current source (referring to BLOCK DIAGRAM). The charging time of C_N, defined as T1, can be calculated as

$$T1 = Cn \times \frac{V_{TH,n}}{I_n} \quad \text{(1)}$$

where $V_{TH,\eta}$ = negative threshold voltage, 1.25V,

In = negative bias current, 5μA

Afterwards, while negative output voltage starts decreasing from 0V, V_{FBN} decreases from 1.1V to 0V proportionally. As V_{FBN} decreases to 10% of V_{REF}, Q7 turns off and Cp starts being charged from 5μA current source (referring to BLOCK DIAGRAM). The charging time of C_P, defined as T2, can be calculated as

$$T2 = Cp \times \frac{V_{TH,P}}{I_P} \quad \text{(2)}$$

where $V_{TH,P}$ = positive threshold voltage, 1.25V

I_P= positive bias current, 5μA

Current Limit And Thermal Protection

To protect devices from damage caused by short circuit, AIC1533 provides current limit and thermal protection. When short circuit occurs, output current is clamped at the current limit. Due to power dissipation of LDO is defined as

$$P_{DISSIPATION} = I_{OUT} * (V_{IN}-V_{OUT}) \quad \text{(3)}$$

Under short circuit condition, the temperature rising, which is caused by power dissipation, gets to thermal shutdown temperature and shuts AIC1533 down. As the temperature gets lower than the thermal shutdown temperature, the device will resume. The pattern of temperature of the device recycles until the short circuit condition is removed. The waveform under short circuit condition is shown as Fig.18.

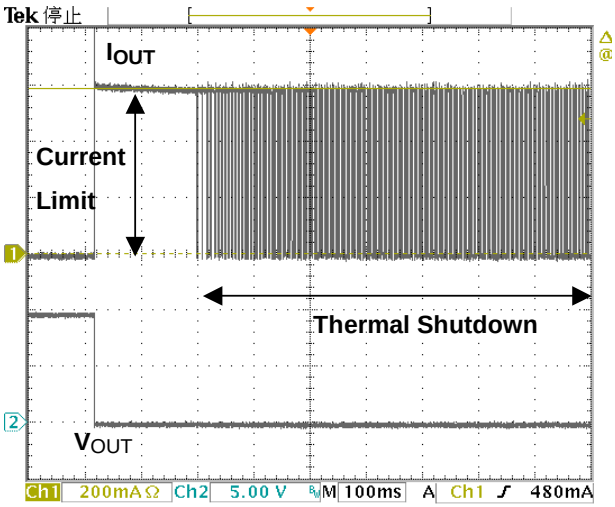


Fig.18 Current Limit Waveform of AIC1533

Shutdown

AIC1533 shuts off all devices and consumes only 0.1μA supple current when $\overline{SHDN}$ gets lower than 0.6V. This pin can be pulled high to 2.4V for normal operation. Due to high impedance of $\overline{SHDN}$ pin, it can't be floating.

Components Selection

1. Determining The Number Of Charge Pump Stages

The number of charge pump stages to regulate is determined by output voltage, supply voltage, switching frequency, load current, forward voltage of diodes, on-resistor of internal MOSFET, and value of ceramic capacitor.

For positive charge pump, the number of required stages can be calculated as

$$N_{POS} \geq \frac{V_{POS} - Vcc + R_{TH} \times Iout}{Vcc - 2V_D} \quad \text{(4)}$$

where V_{POS} = output of positive charge pump

R_{TH} = equivalent output impedance of charge pump

V_D = forward voltage of diodes

Vcc = input voltage

The following equation approximates R_{TH}

$$R_{TH} = 2(R_{DS,ON(P)} + R_{DS,ON(N)}) + (\frac{1}{C_{FLY} \times F_{SW}}) + (\frac{1}{C_O \times F_{SW}}) \quad \text{(5)}$$

where $R_{DS,\ ON(P)}$ is on-resistor of internal P-channel MOSFET, $R_{DS,\ ON(N)}$ means on-resistor of internal N-channel MOSFET, and F_{SW} is switching frequency of AIC1533 (***referring to*** **ELECTRIVAL CHARACTERISTICS**).

For negative charge pump, the number of negative charge pump can be determined by

$$N_{NEG} \geq \frac{R_{TH} \times Iout - V_{NEG}}{Vcc - 2V_D} \quad (6)$$

where V_{NEG} = output of negative charge pump

Example

To obtain V_{POS}=28V/30mA, V_{NEG}=-9V/30mA from V_{CC}=12V, C_{FLY}=0.1μF, the number of positive and negative charge pumps can be calculated as follows

$$R_{TH} = 2(R_{DS,ON(P)} + R_{DS,ON(N)}) + (\frac{1}{C_{FLY} \times F_{SW}}) + (\frac{1}{C_O \times F_{SW}})$$

$$= 2(10+10) + (\frac{1}{0.1\times10^{-6} \times 1\times10^{6}}) + (\frac{1}{1\times10^{-6} \times 1\times10^{6}})$$

$$=51 \quad (7)$$

$$N_{POS} \geq \frac{V_{POS} - Vcc + R_{TH} \times Iout}{Vcc - 2V_D} = \frac{28 - 12 + (51\times 30\times 10^{-3})}{12 - 2\times 0.5} = 1.59 \quad (8)$$

$$N_{NEG} \geq \frac{R_{TH} \times Iout - V_{NEG}}{Vcc - 2V_D} = \frac{(51\times 30\times 10^{-3}) - (-9)}{12 - 2\times 0.5} = 0.96 \quad (9)$$

Thus, the number of positive charge pump is two, and the negative one requires one charge pump.

2. Output Voltage Selection

2.1 Output voltage of LDO

A resistor divider, determining output voltage of LDO, connects to OUT, GND, and ADJ (referred to TYPICAL APPLICATION CIRCUIT). Values of resistors can be calculated by equation (10).

$$V_{LDO} = V_{ADJ} \times (1 + \frac{R3}{R4}) \quad (10)$$

where V_{LDO} = output voltage of LDO

V_{ADJ} = adjustable voltage of LDO, the recommended R4 is 130kΩ.

2.2. Output Voltage Of Positive Charge Pump

Output voltage of positive charge pump is determined by connecting a resistor divider to output terminal of positive charge pump, GND, and FBP (***referred to*** **TYPICAL APPLICATION CIRCUIT**). The values of resistor divider can be calculated as equation (11).

$$V_{POS} = V_{FBP} \times (1 + \frac{R1}{R2}) \quad (11)$$

where V_{POS} = output voltage of positive charge pump

V_{FBP} = feedback voltage of positive charge pump, 1.25V. The recommended R2 is 22kΩ

2.3 Output voltage of negative charge pump

Since comparator input of negative charge pump, FBN, is referenced to 0V, a positive reference voltage, which can be obtained by adding a 0.22μF bypass capacitor between VREF and GND, is needed (***referred to*** **TYPICAL APPLICATION CIRCUIT**). The value of resistor dividers can be calculated as equation (12).

$$V_{NEG} = -V_{REF} \times \frac{R5}{R6} \quad (12)$$

where V_{NEG} represents output voltage of negative charge pump, and V_{REF} means reference voltage, 1.25V. The recommended R6 is 33kΩ.

3. Flying Capacitor Selection

A flying capacitor plays an important role in charge pump strength. Increase of flying capacitor value results in a rise of output capability with smaller ripple voltage. Normal voltage of flying capacitor must comply with the following conditions, as equation (13).

$V_{CFLY\ (POS)} = V_{CFLY\ (NEG)} > 1.5 \times [V_{CC} \times (N)]$ .....(13)

Where $V_{CFLY(POS)}$ is the normal voltage of positive charge pump flying capacitor, $V_{CFLY(NEG)}$ represents the normal voltage of negative charge pump flying capacitor, and N means the number of charge pump stages

Besides, ceramic capacitors composed by different materials, such as X7R, X5R, Z5U and Y5V, have different tolerance in temperature, and result in different capacitance loss. A capacitor, which is made of X7R or X5R, is recommended for AIC1533 applications.

4. Input-Output Capacitor Selection

4.1 LDO

AIC1533 needs input and output capacitors to maintain stability. The recommended values for both input and output capacitors are 10μF. Because of the material, X5R or X7R, ceramic capacitor has low ESR and excellent electrical characteristics in over temperature. That makes ceramic capacitor suitable for output and input capacitors of AIC1533.

4.2 Charge Pump

A ceramic capacitor of a value, which is 10 times of flying capacitor, is suitable for the output capacitor of charge pump. In order to maintain a stable output voltage, make sure to place the capacitor as close to IC as possible.

5. Rectifier Diode Selection

A Schottky diode with a current rating equal to or greater than two times of average charge pump input current, and a voltage rating at least 1.5 times of V_{CC}, is recommended.

Table 1 indicates the recommended components for AIC1533 applications.

Table.1 Bill of Materials List

Designator	Part Type	Description	Vender	Phone
C_{IN}	10μF/16V	Ceramic capacitor, EMK325BJ106MN-B	Taiyo Yuden	02-27972155-314
C_{FLY1}	0.1μF/50V	Ceramic capacitor, UMK212BJ104KG	Taiyo Yuden	02-27972155-314
C_{FLY2}	0.1μF/50V	Ceramic capacitor, UMK212BJ104KG	Taiyo Yuden	02-27972155-314
C_{FLY3}	0.1μF/16V	Ceramic capacitor, EMK107BJ104KA	Taiyo Yuden	02-27972155-314
C_{O1}	1μF/50V	Ceramic capacitor, UMK212F105ZG	Taiyo Yuden	02-27972155-314
C_{O2}	1μF/16V	Ceramic capacitor, EMK212F105KG	Taiyo Yuden	02-27972155-314
C_{O3}	10μF/16V	Ceramic capacitor, EMK325BJ106MN-B	Taiyo Yuden	02-27972155-314
D1~D3	BAT54SW	Surface mount Schottky barrier diode	WTE	07-8225408
U1	AIC1533	Triple Adjustable Output DC/DC Converter with a LDO	AIC	03-5772500

Layout Consideration

Due to the switching frequency of AIC1533, careful PCB layout is necessary. Place components as close to one another as possible and maintain each connection of minimum length and maximum width of trace for best performance. Make sure each device connect to its immediate ground plane. Fig 19, 20 and 21 represent recommended layouts.

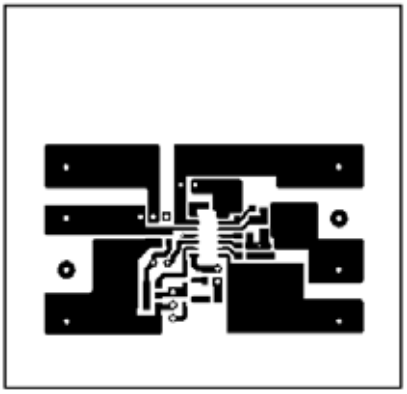


Fig. 19 Top Layer

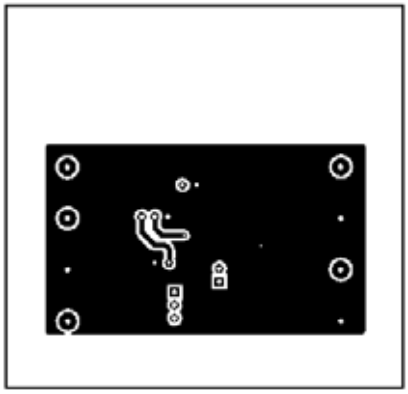


Fig. 20 Bottom Layer

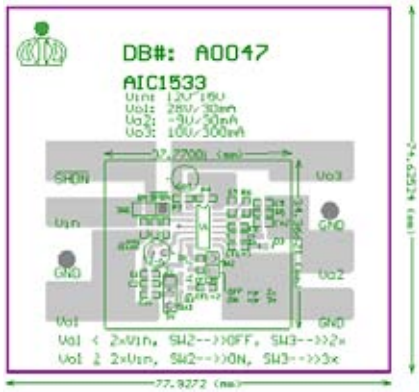
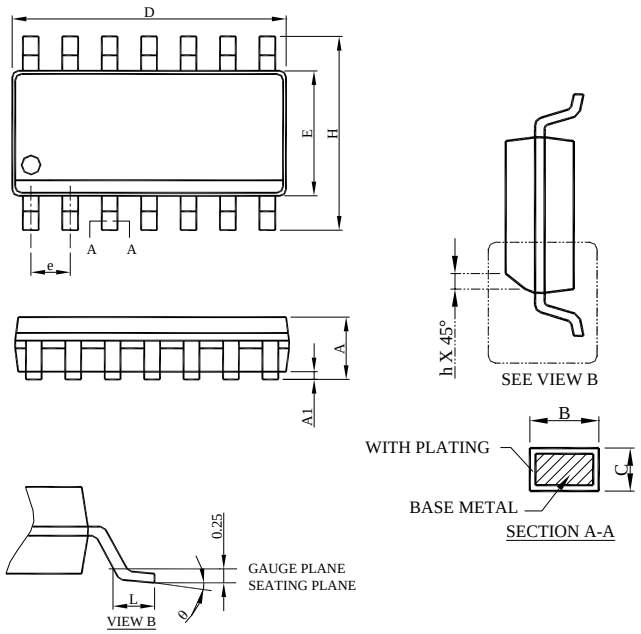


Fig. 21 Top-over Layer

PHYSICAL DIMENSIONS (unit: mm)

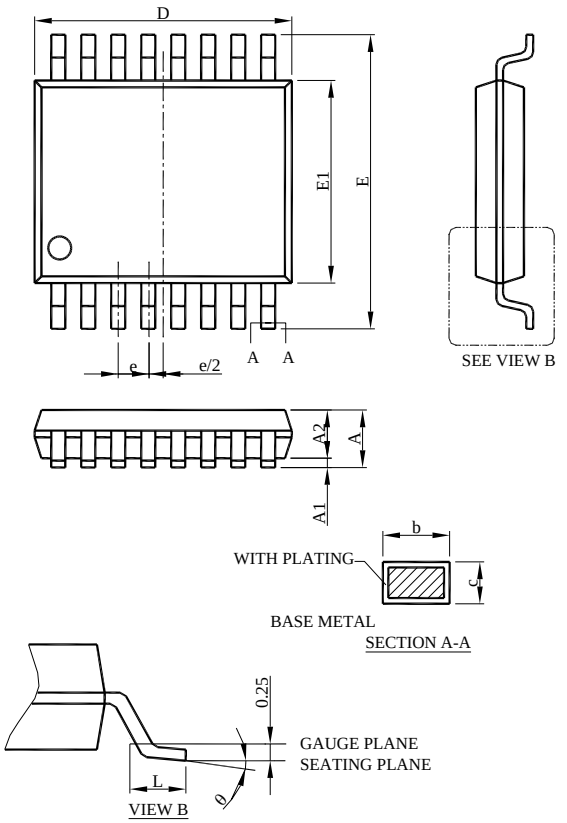
- **SOP-14**



SYMBOL	SOP-14	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	8.55	8.75
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note:
1.Refer to JEDEC MS-012AB.
2.Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3.Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash or protrusion shall not exceed 10 mil per side.
4.Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

- **TSSOP-16**



SYMBOL	TSSOP-16	
	MILLIMETERS	
	MIN.	MAX.
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75
θ	0°	8°

Note:
1. Refer to JEDEC MO-153AB.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Note: