Shanghai Fudan Microelectronics Group Company Limited

复旦微电子

FM29G04C
3V 4G-BIT NAND FLASH MEMORY

Datasheet

Jun. 2018

Trademarks

Features Summary

- **Voltage Supply**
  - Vcc: 2.7V ~ 3.6V
- **Operation Temperature**
  - -40℃~85℃
- **Organization**
  - Single-level cell (SLC) technology
  - Memory Cell Array: (512M+16M) x 8bit
  - Data Register : 2112 bytes (2048 + 64 bytes)
- **Automatic Program and Erase**
  - Page Program : 2112 bytes (2048 + 64 bytes)
  - Block size : (128K + 4K) bytes
- **Page Read Operation**
  - Page size : 2112 bytes (2048 + 64 bytes)
  - Random Read: 25μs (Max.)
  - Serial Access: 25ns (Min.)
  - Data Transfer Rate: SDR 40MHz (40MB/s)
- **Program/Erase/Read Speed**
  - Page Program time : 400μs (Typ.)
  - BLOCK ERASE time : 4.5ms (Typ.)
- **Command/Address/Data Multiplexed I/O Port**
- **Hardware Data Protection**
  - Program/Erase Lockout during Power Transitions
- **Reliability**
  - Endurance : 100,000 Program/Erase Cycles
  - Data retention: 10 years
- **Command Driven Operation**
- **Package**
  - TSOP48 (12X20mm)
  - All Packages are RoHS Compliant and Halogen-free

1. Summary Description

FM29G04C is offered in 3.3V Vcc with x8 I/O interface. Its NAND cell provides the most cost-effective solution for solid state application market. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

1.1. Packaging Type and Pin Configurations

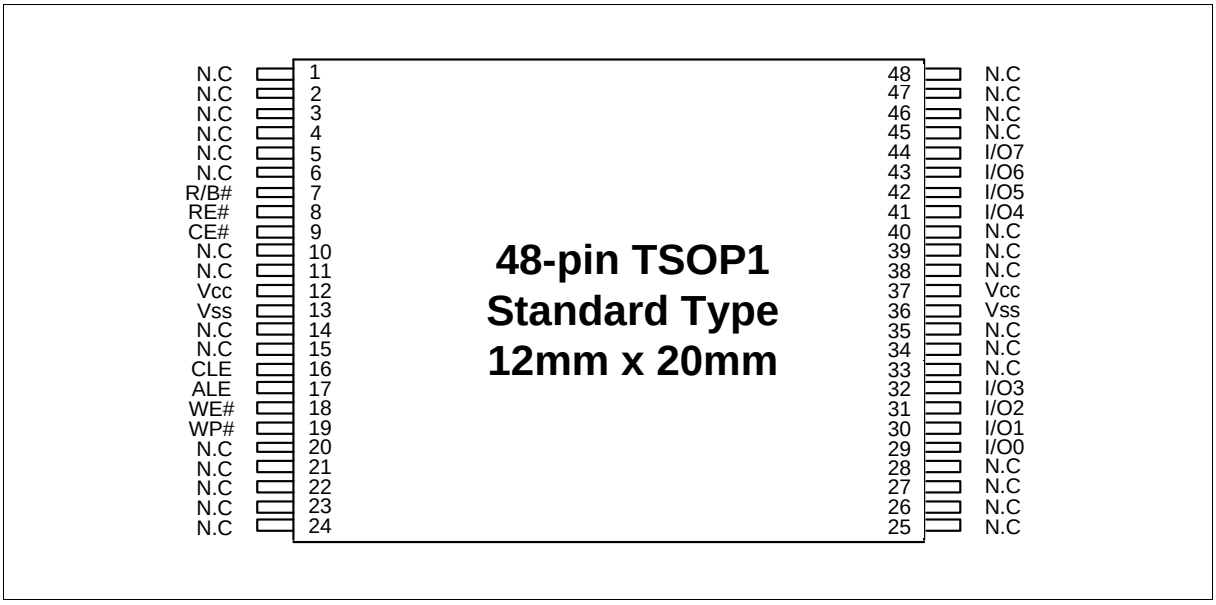


Figure 1 FM29G04C pad assignments, TSOP48

1.2. Pin Description

Pin Name	FUNCTION
I/O0~I/O7	**Data Inputs/Outputs** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**Command Latch Enable** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	**Address Latch Enable** The ALE input controls the activating path for address to the internal address register. Addresses are latched on the rising edge of WE# with ALE high.
CE#	**Chip Enable** The CE# input is the device selection control. When the device is in the Busy State, CE# high is ignored, and the device does not return to standby mode in program or erase operation.
RE#	**Read Enable** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.

Pin Name	FUNCTION
WE#	**Write Enable** The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**Write Protect** The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**Ready/Busy Output** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
Vcc	**Power** Vcc is the power supply for device.
Vss	**Ground**
N.C	**No connection**

NOTE:

1. Connect all Vcc and Vss pins of each device to common power supply outputs.

1.3. Block Diagram

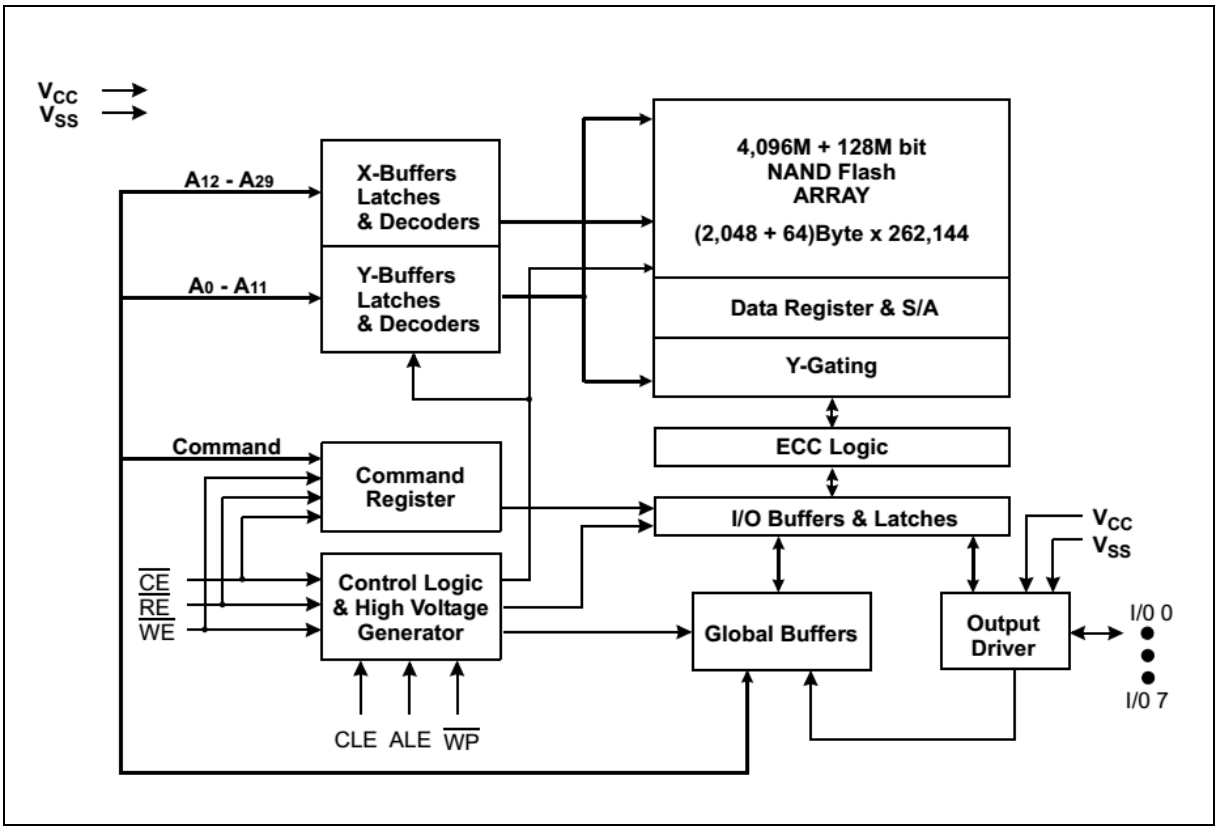
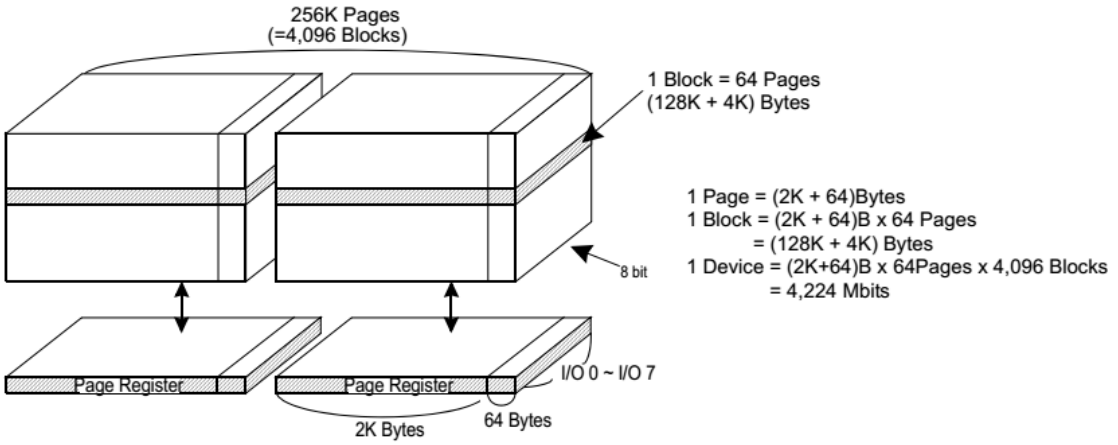


Figure 2 FM29G04C NAND Flash Memory Block Diagram

1.4. Memory Mapping



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	**Column Address**
3rd Cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	**Row Address**
4th Cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	**Row Address**
5th Cycle	A_{28}	A_{29}	*L	*L	*L	*L	*L	*L	**Row Address**

Figure 3 FM29G04C Memory Map

NOTE:
1. Column Address: Starting Address of the Register.
2. *L must be set to Low
3. *The device ignores any addition input of address cycle than required.

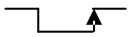
1.5. Command Set

Table 1 Command Set

Function	1st Cycle	2nd Cycle	Accept Command during Busy
Read(3)	00h	30h	
Read for copy back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Two-Plane Page Program(2)	80h-11h	81h-10h	
Copy-Back Program	85h	10h	
Two-Plane Copy-Back Program(2)	85h-11h	81h-10h	
Block Erase	60h	D0h	
Two-Plane Block Erase	60h-60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Read Status	70h		O
ECC Read Status	7Ah		

NOTE:
1. Random Data Input/Output can be executed in a page.
2. Any command between 11h and 81h is prohibited except 70h and FFh.
3. Command 80h + Address 1cycle must be inserted before the Read CMD(00h-30h).

1.6. Mode Selection

Mode		CLE	ALE	CE#	WE#	RE#	WP#
Read Mode	Command Input	H	L	L		H	X
	Address Input (5cycle)	L	H	L		H	X
Write Mode	Command Input	H	L	L		H	H
	Address Input (5cycle)	L	H	L		H	H
Data Input		L	L	L		H	H
Data Output		L	L	L	H		X
During Read (Busy)		X	X	X	X	H	X
During Program (Busy)		X	X	X	X	X	H
During Erase (Busy)		X	X	X	X	X	H
Write Protect		X	X(1)	X	X	X	L
Stand-by		X	X	H	X	X	0V/Vcc(2)

NOTE:
1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

2. Electrical Characteristics

2.1. Valid Block

Parameter	Symbol	Min	Typ	Max	Unit
FM29G04C	N_{VB}	4,016	-	4,096	Block

2.2. Recommended Operation Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	Vcc	2.7	3.3	3.6	V
Ground Supply Voltage	Vss	0	0	0	V

2.3. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V_{CC}	-0.6 to 4.6	V
	V_{IN}	-0.6 to 4.6	
	$V_{I/O}$	-0.6 to Vcc+0.3（<4.6V）	
Temperature Under Bias	T_{BIAS}	-40 to +85	°C

NOTE:

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.
3. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.4. DC And Operating Characteristics

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	Icc1	t_{RC}=50ns, CE#=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	Icc2	-				
	Erase	Icc3	-				
Standby Current (TTL)		I_{SB1}	CE#=V_{IH}, WP#=0V/Vcc	-	-	1	
Standby Current(CMOS)		I_{SB2}	CE#=Vcc-0.2, WP#=0V/Vcc	-	10	70	μA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±10	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	
Input High voltage		V_{IH}	-	0.8×Vcc	-	Vcc+0.3	V
Input Low voltage		V_{IL}	-	-0.3	-	0.2×Vcc	
Output High voltage Level		V_{OH}	I_{OH}=-400uA	2.4	-	-	
Output Low voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/B#)		I_{OL} (R/B#)	V_{OL}=0.4V	8	10	-	mA

NOTE:

1. VIL can undershoot to -0.4V and V_{IH} can overshoot to VCC +0.4V for duration of 20ns or less.
2. Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

2.5. AC Test Condition

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF

2.6. Capacitance

(TA=25°C, VCC=3.3V, f=1.0MHz)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IL}=0V	-	8	pF

NOTE:
1. Capacitance is periodically sampled and not 100% tested.

2.7. Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	t_R	-		25	μs
Program Time	t_{PROG}	-	400	900	μs
Dummy Busy Time for Two-Plane Page Program	t_{DBSY}	-	0.5	1	μs
Number of Partial Program Cycles	N_{OP}	-	-	1	cycles
Block Erase Time	t_{BERS}	-	4.5	16	ms

NOTE:
1. Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.
2. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25°C temperature.

2.8. AC timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t_{CLS}(1)	12	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
CE# Setup Time	t_{CS}(1)	20	-	ns
CE# Hold Time	t_{CH}	5	-	ns
WE# Pulse Width	t_{WP}	12	-	ns
ALE Setup Time	t_{ALS}(1)	12	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	t_{DS}	12	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	25	-	ns
WE# High Hold Time	t_{WH}	10	-	ns
Address to Data Loading Timing	t_{ADL}(2)	70	-	ns
ALE to RE# Delay	t_{AR}	10	-	ns
CLE to RE# Delay	t_{CLR}	10	-	ns
Ready to RE# Low	t_{RR}	20	-	ns
RE# Pulse Width	t_{RP}	12	-	ns
WE# High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	25	-	ns
RE# Access Time	t_{REA}	-	20	ns
CE# Access Time	t_{CEA}	-	25	ns
RE# High to Output Hi-Z	t_{RHZ}	-	100	ns
CE# High to Output Hi-Z	t_{CHZ}	-	30	ns
CE# High to ALE or CLE Don't Care	t_{CSD}	0	-	ns
RE# High to Output Hold	t_{RHOH}	15	-	ns
RE# Low to Output Hold	t_{RLOH}	5	-	ns
CE# High to Output Hold	t_{COH}	15	-	ns
RE# High time	t_{REH}	10	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	ns
RE# High to WE# Low	t_{RHW}	100	-	ns
WE# High to RE# Low	t_{WHR}	60	-	ns
Device Reset Time (Read/Program/Erase)	t_{RST}(3)	-	5/10/500(3)	μs

NOTE:
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
3. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

3. Timing Diagram

3.1. Command Latch Cycle

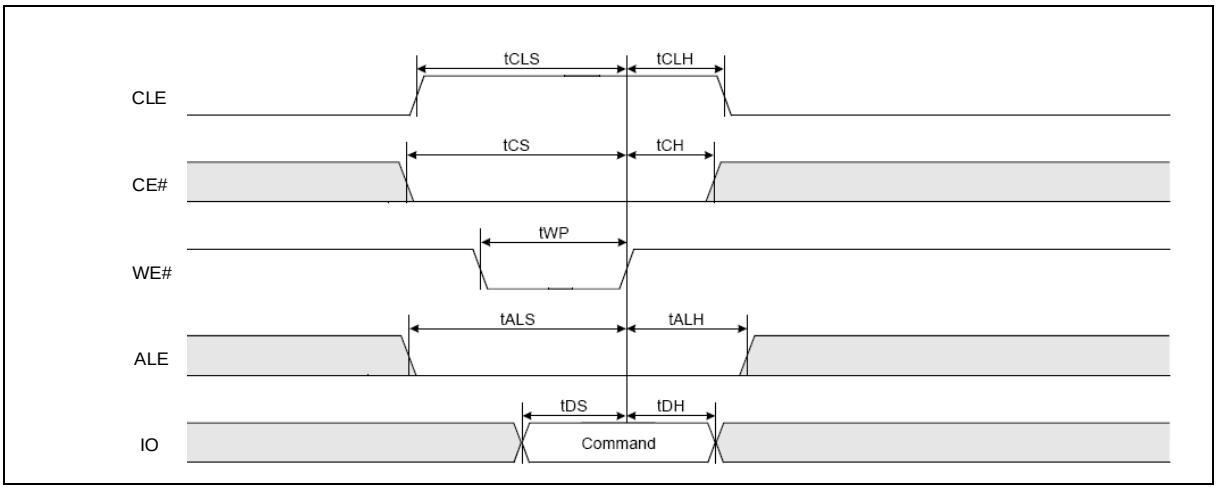


Figure 4 Command Latch timing

3.2. Address Latch Cycle

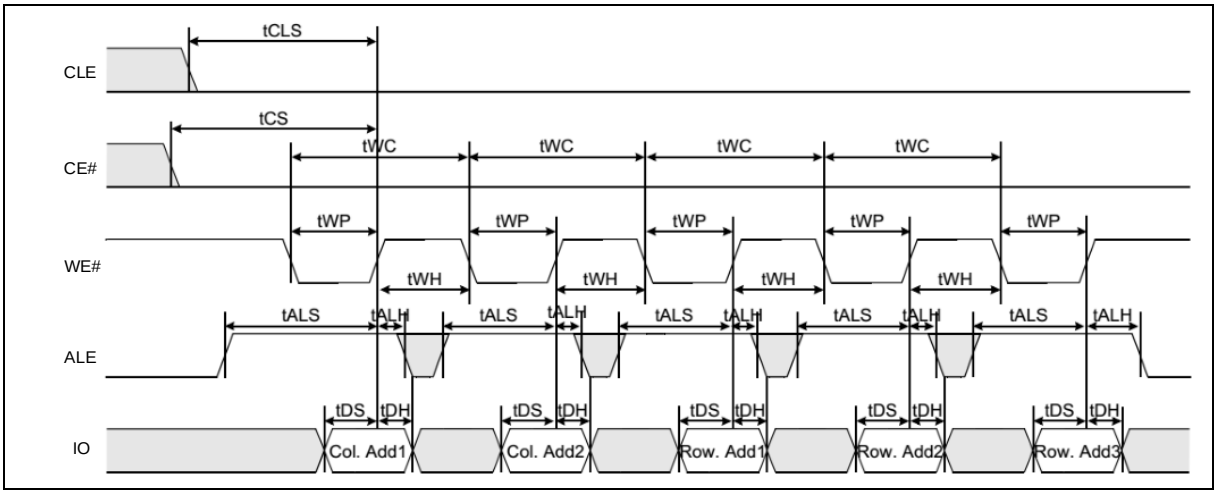


Figure 5 Address Latch timing

3.3. Input Data Latch Cycle

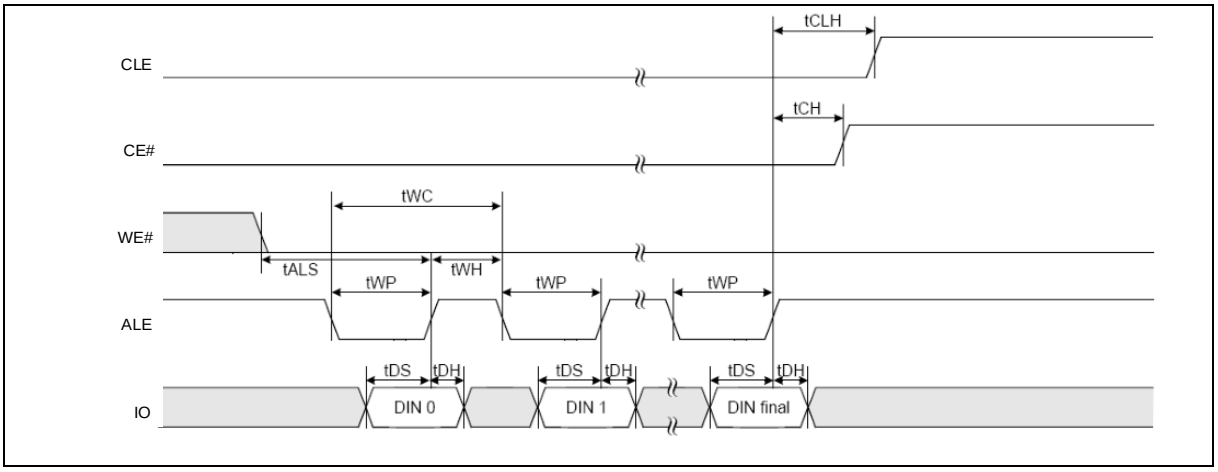


Figure 6 Input Data Latch timing

3.4. Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

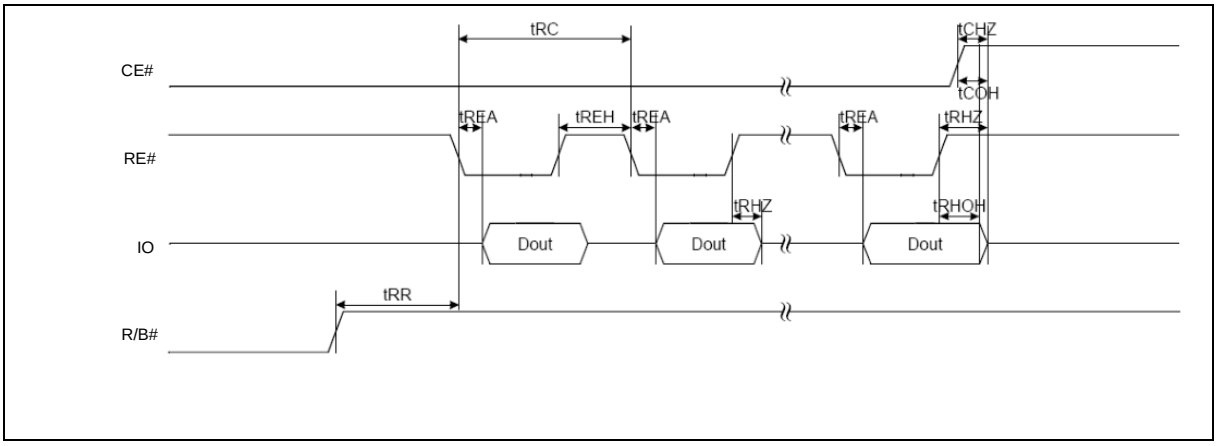


Figure 7 Serial Read timing

NOTE:

1. Transition is measured at ±200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

3.5. Status Read Cycle

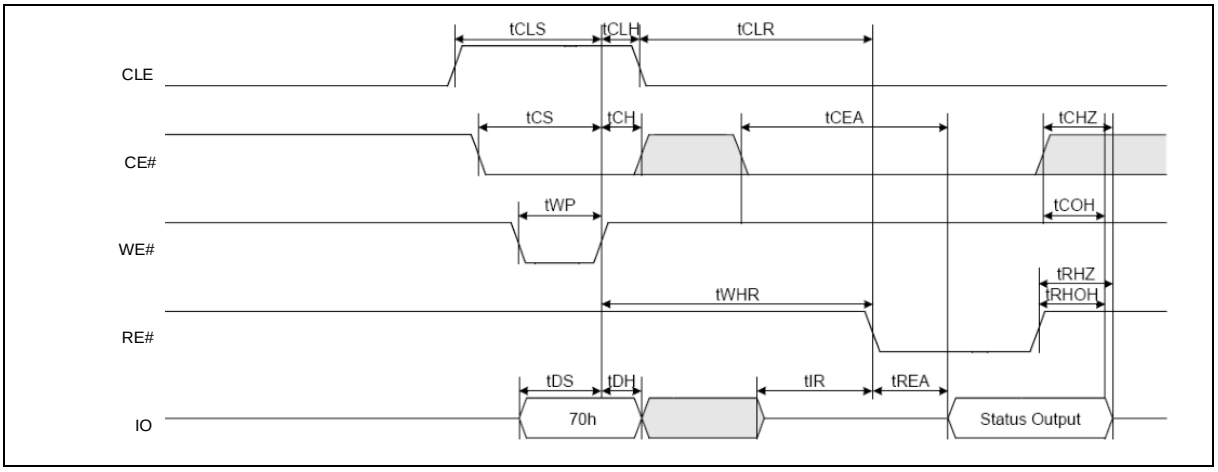


Figure 8 Status Read timing

3.6. ECC Status Read Cycle

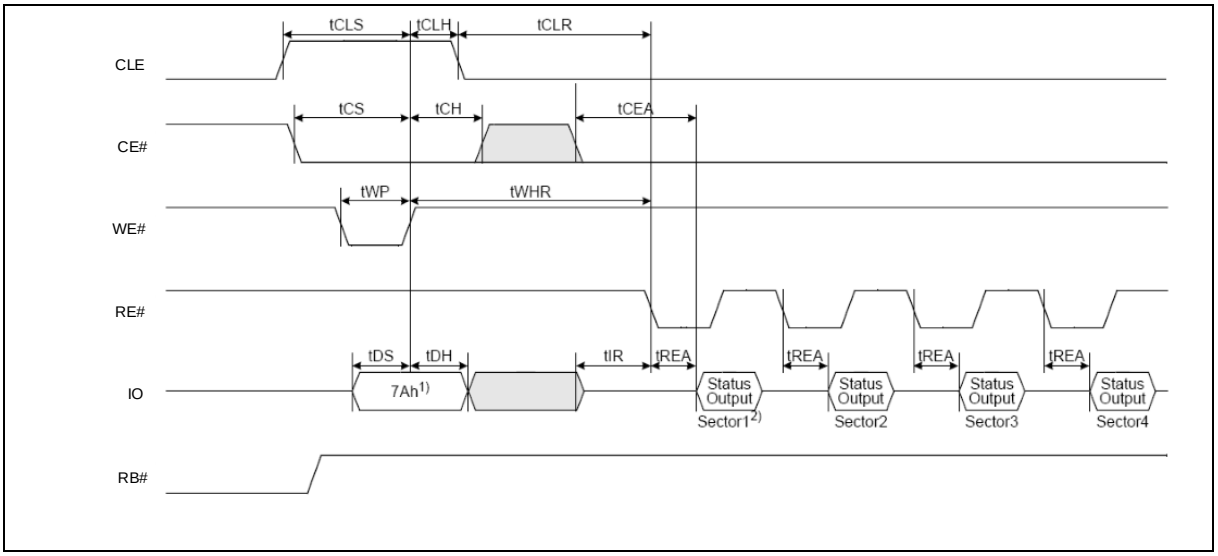


Figure 9 ECC Status Read timing

NOTE:

1. ECC Status output should include all 4 sector information.

3.7. Read Operation

Command 80h + Address 1cycle must be inserted before the Read Operation.

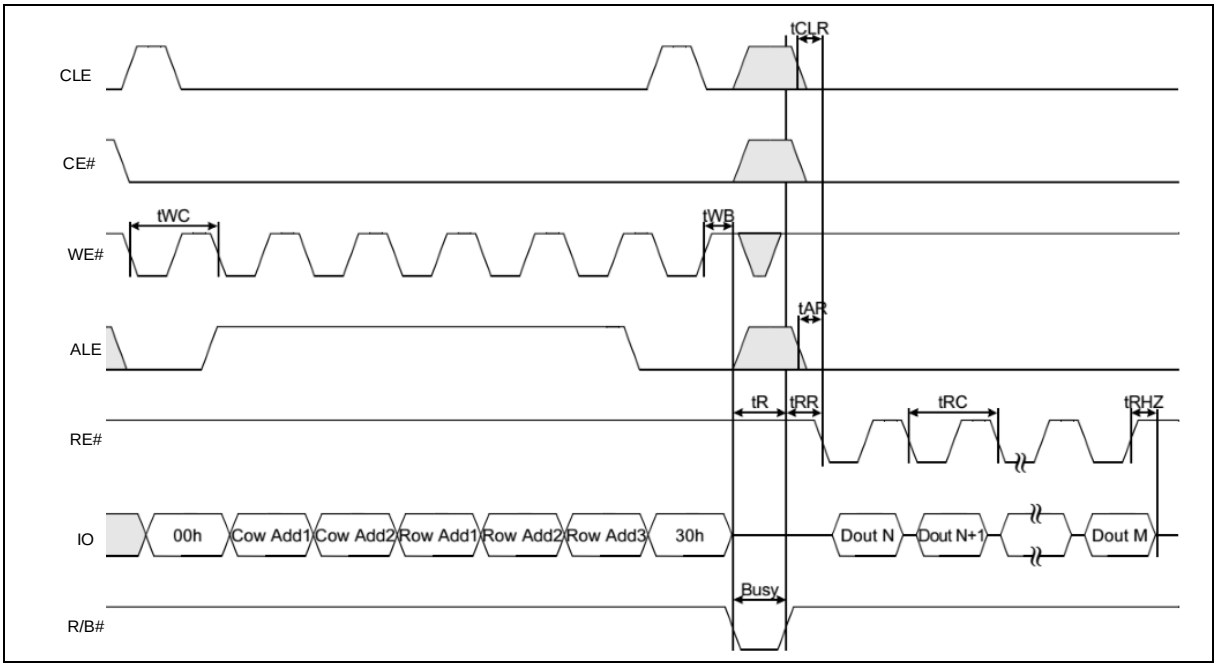


Figure 10 Read operation

3.8. Read Operation (Intercepted by CE#)

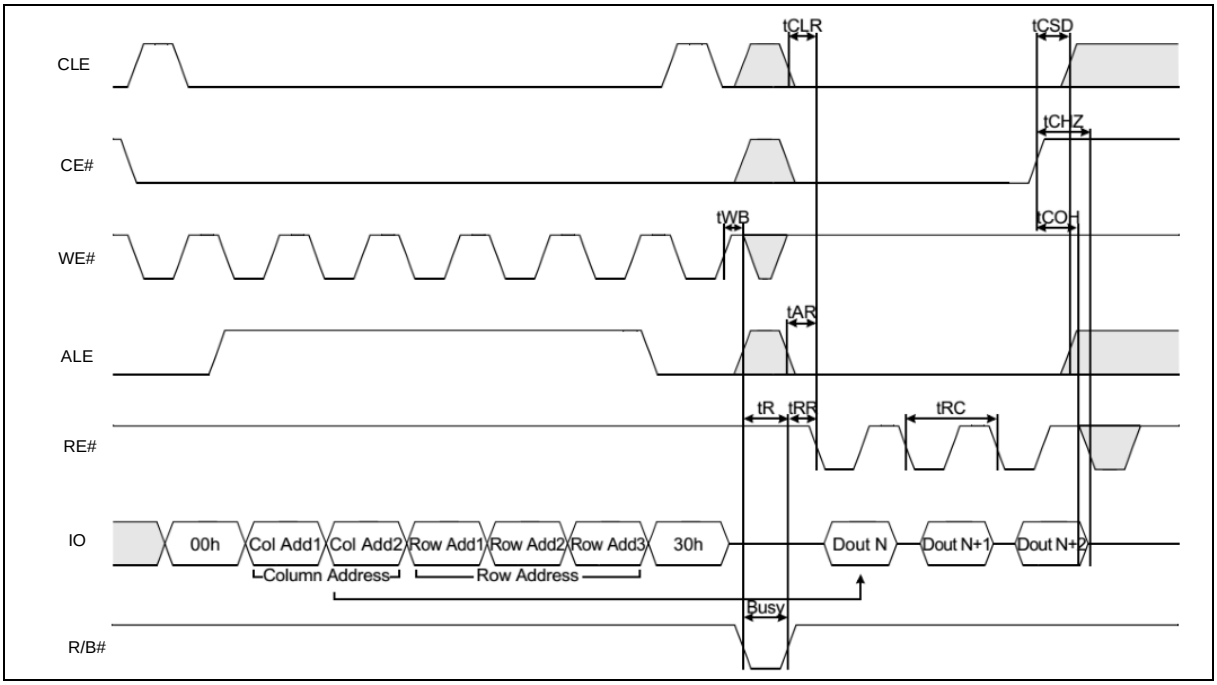


Figure 11 Read Operation (Intercepted by CE#)

3.9. Random Data Output In a Page Operation

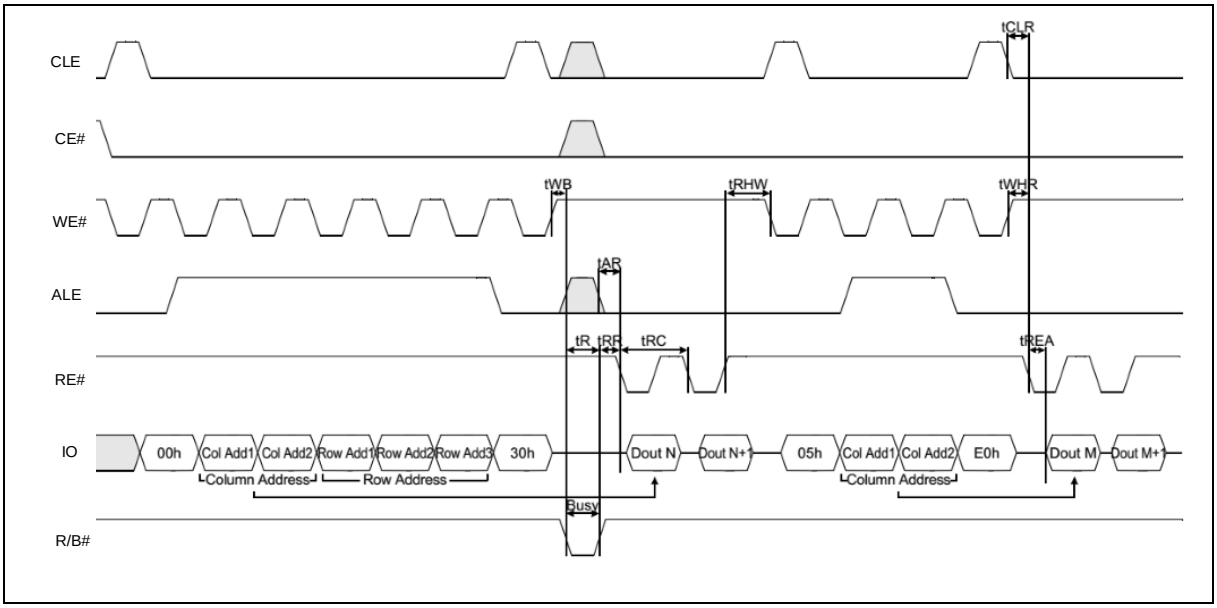


Figure 12 Random Data Output In a Page Operation

3.10. Page Program Operation

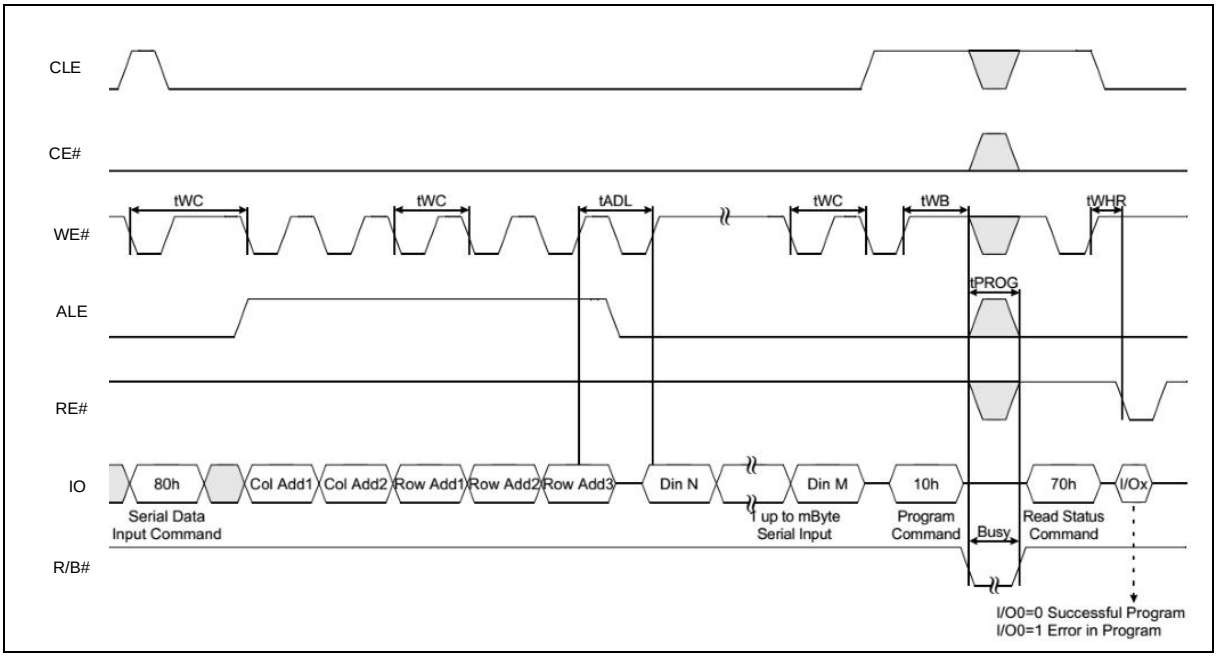
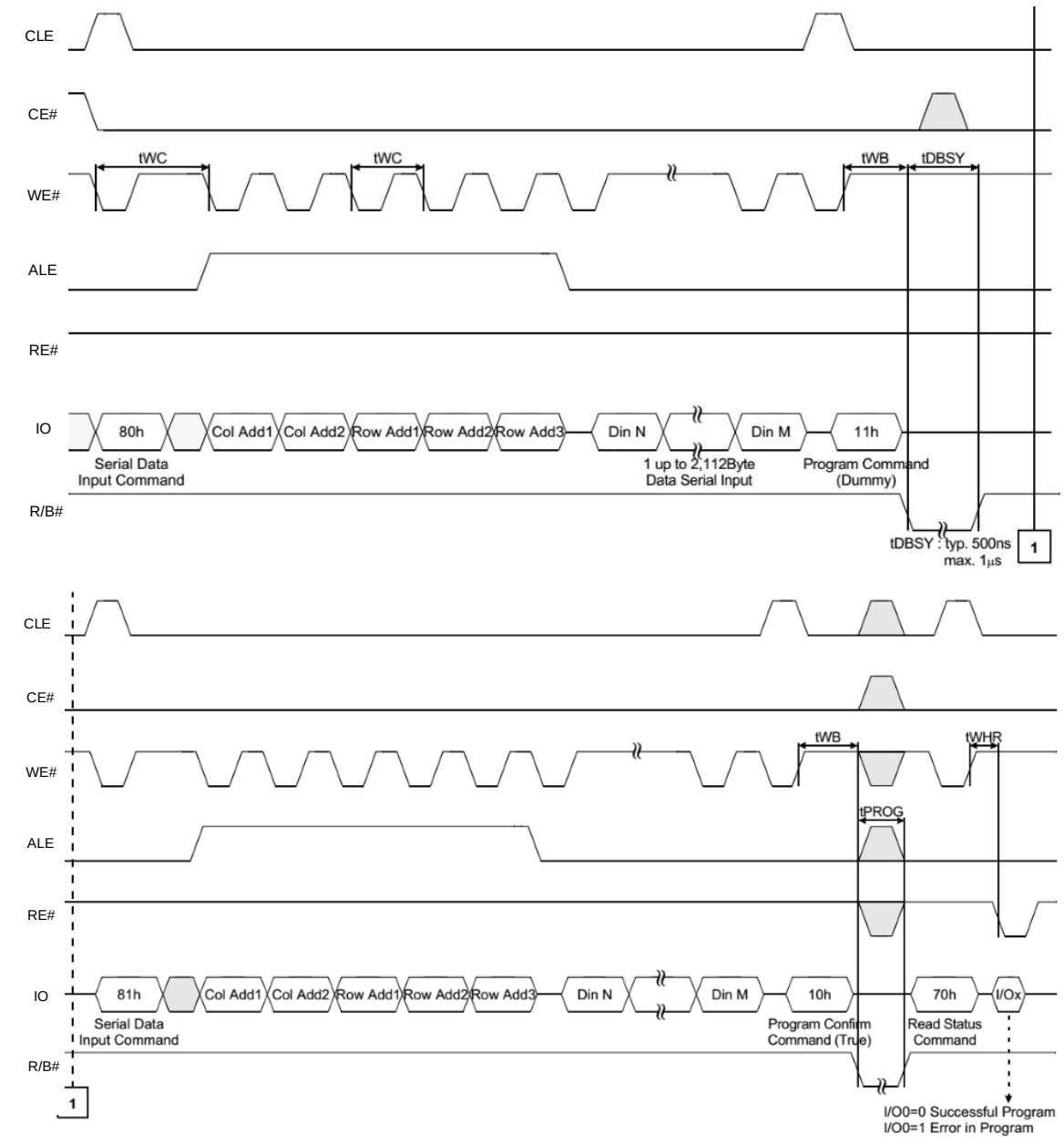


Figure 13 Page Program Operation

NOTE:

1. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

3.11. Two-Plane Page Program Operation



NOTE:

1) Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 14 Two-Plane Page Program Operation

3.12. Page Program Operation with Random Data Input

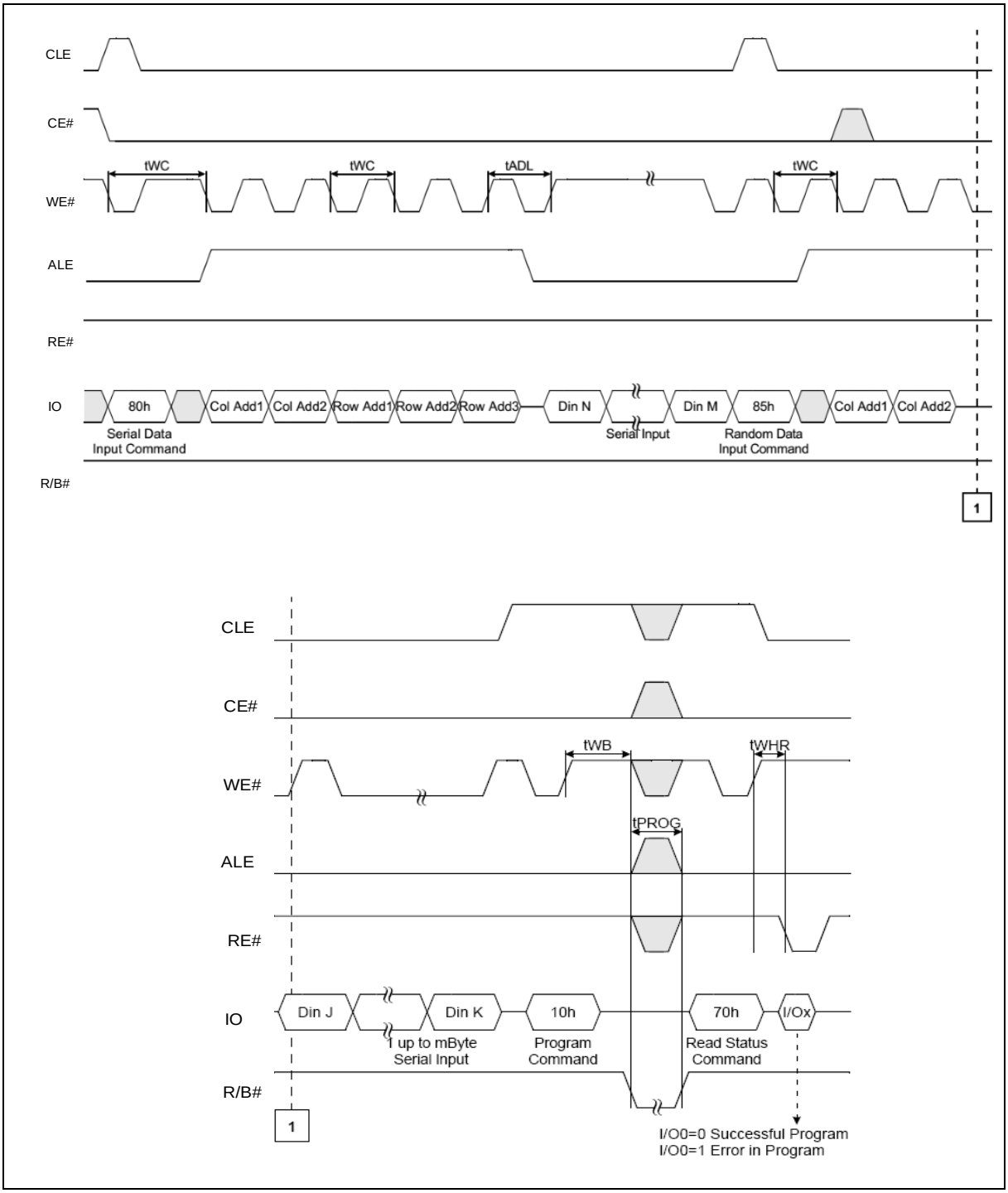


Figure 15 Page Program Operation with Random Data Input Operation

3.13. Copy-Back Program Operation

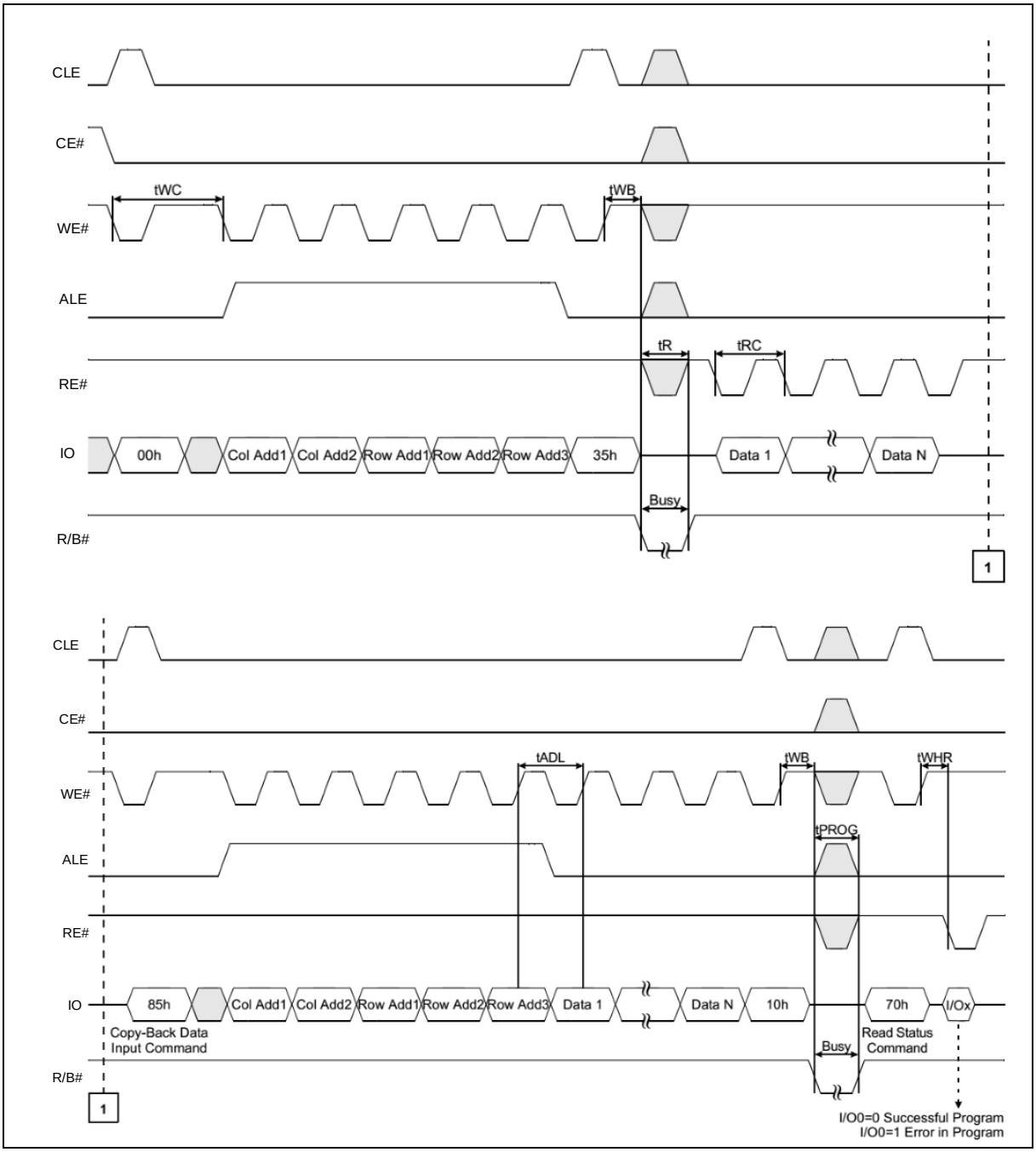


Figure 16 Copy-Back Program operation

3.14. Two-Plane Copy-Back Program Operation(1/2)

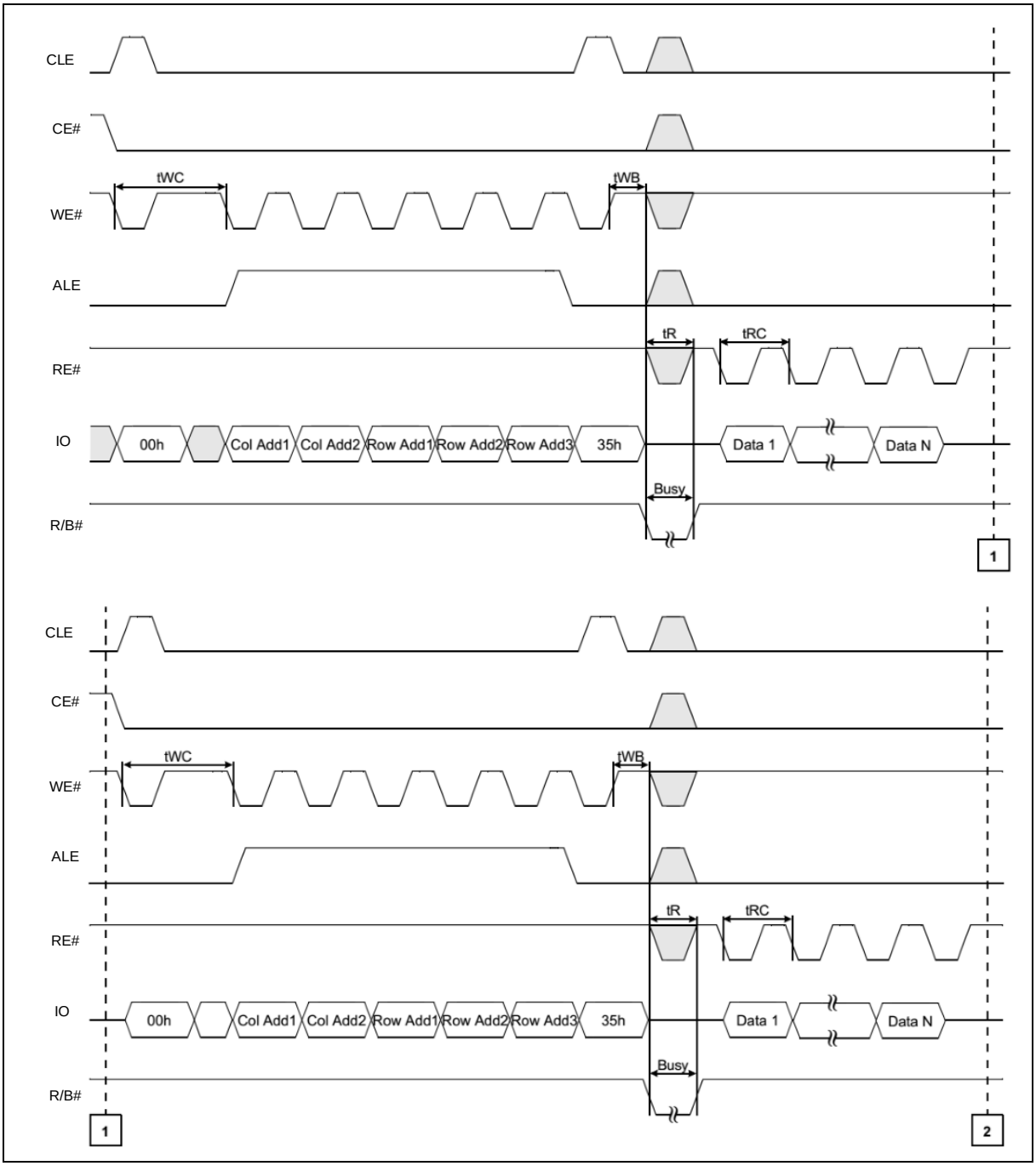
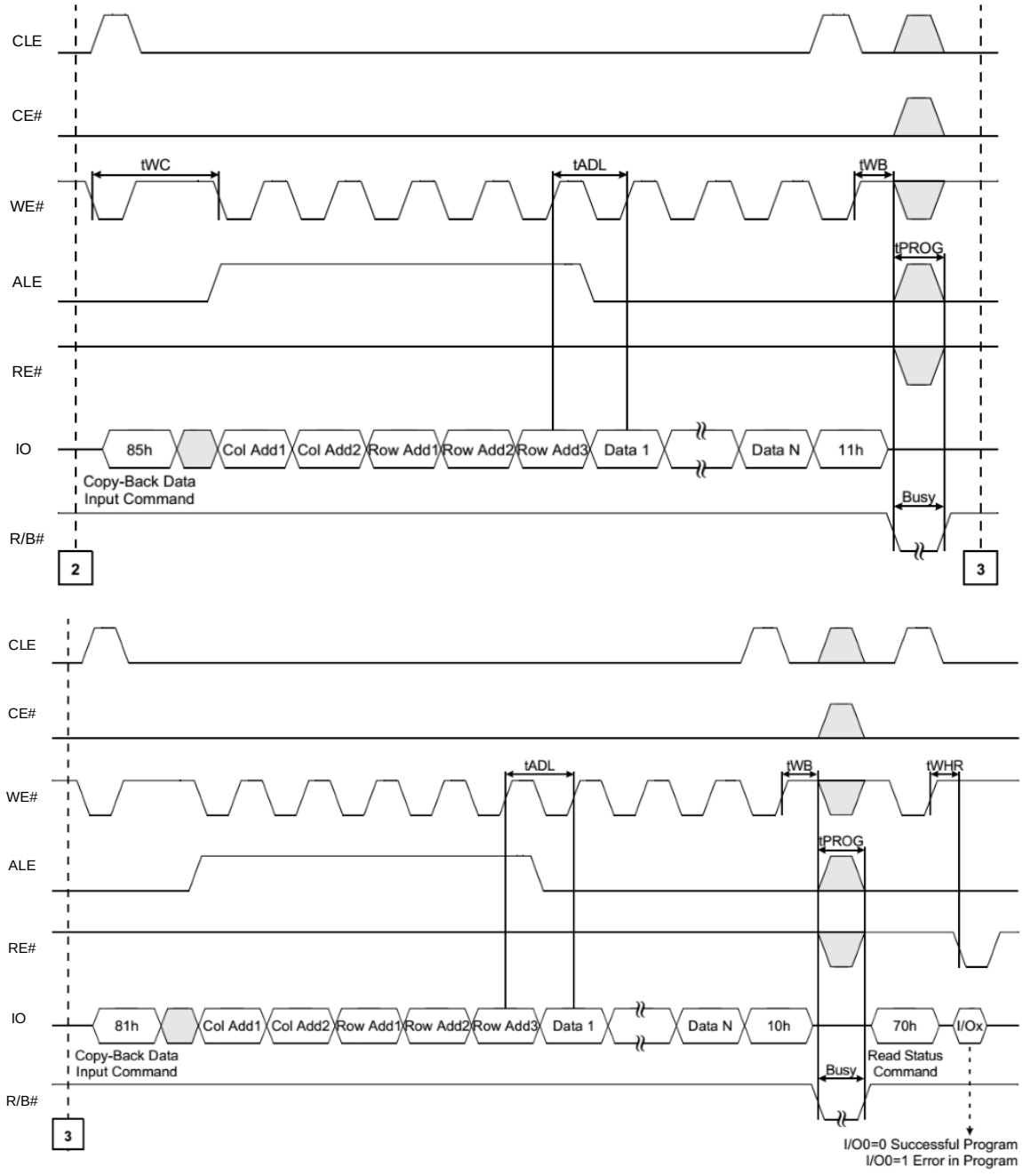


Figure 17 Copy-Back Program operation

3.15. Two-Plane Copy-Back Program Operation(2/2)

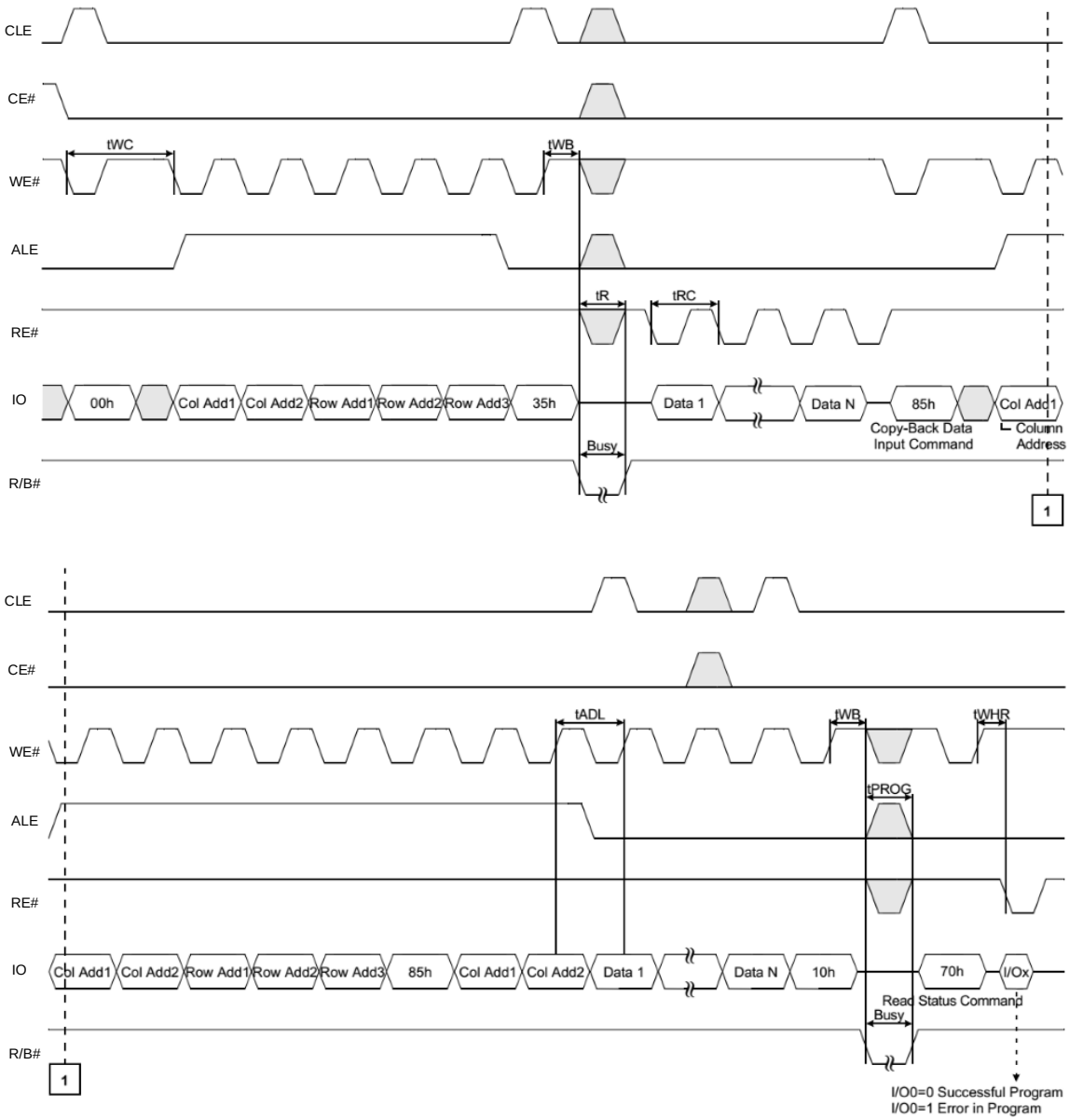


NOTE:

1) t_{ADL} is the time from the WE# rising edge of the final address cycle to the WE# rising edge of the first data cycle.

Figure 18 Two-Plane Copy-Back Program operation

3.16. Copy-Back Program Operation with Random Data Input



NOTE:

1) t_{ADL} is the time from the WE# rising edge of the final address cycle to the WE# rising edge of the first data cycle.
2) Copy-Back Program operation is allowed only within the same memory plane.

Figure 19 Copy-Back Program operation with Random Data Input

3.17. Block Erase Operation

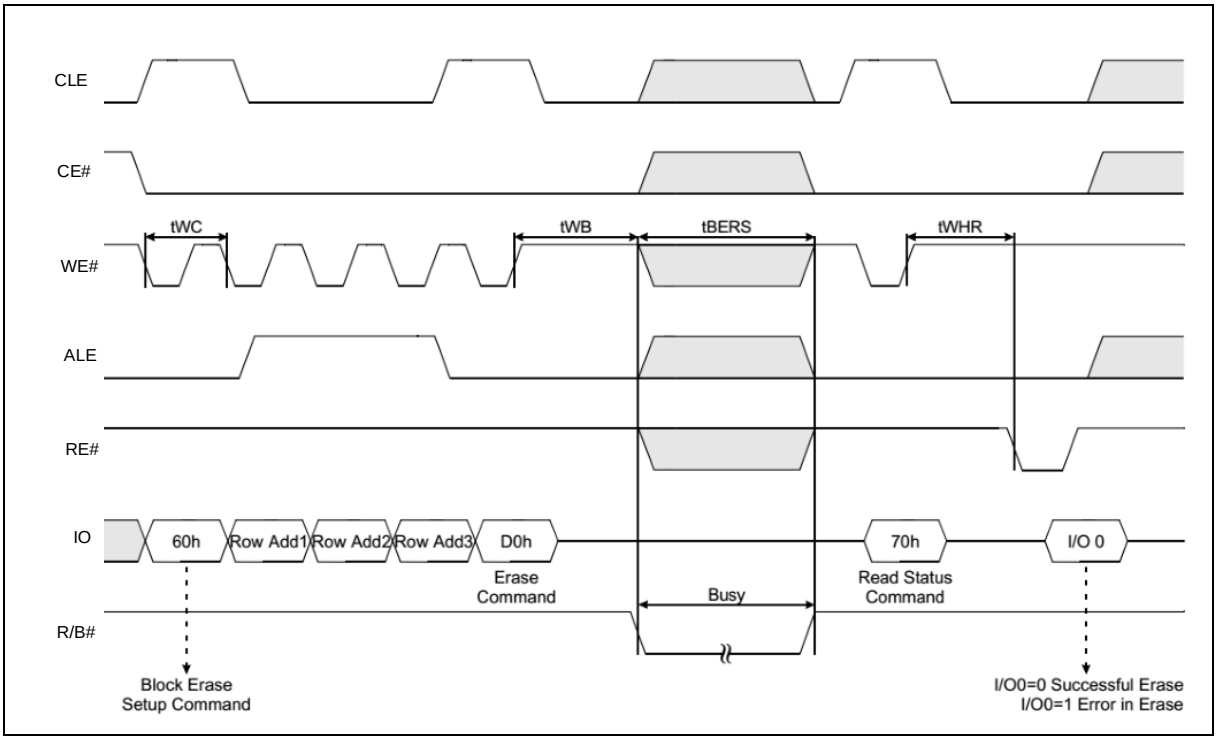


Figure 20 Block Erase operation

3.18. Two-Plane Block Erase Operation

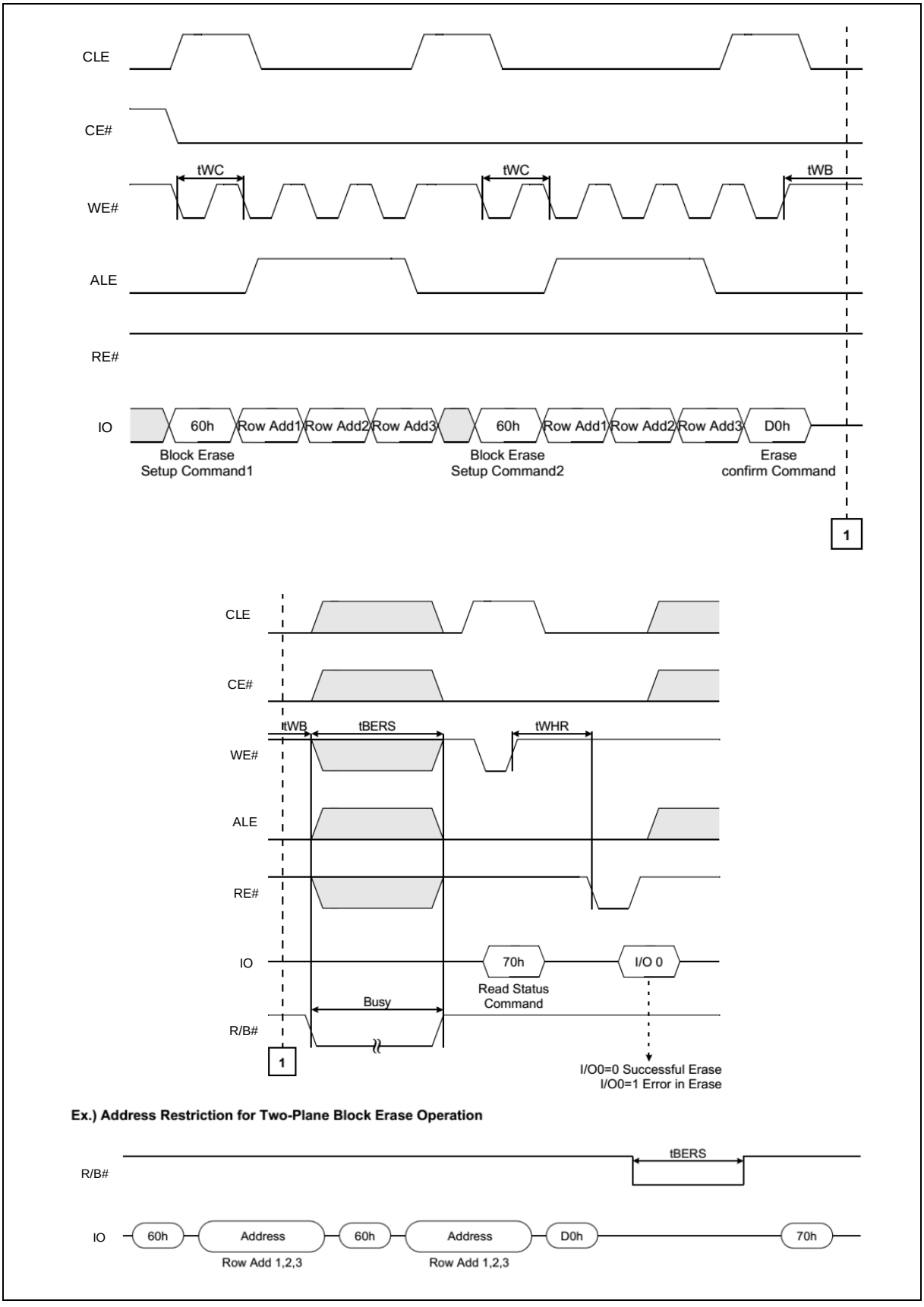


Figure 21 Two Plane Block Erase operation

3.19. Read ID Operation

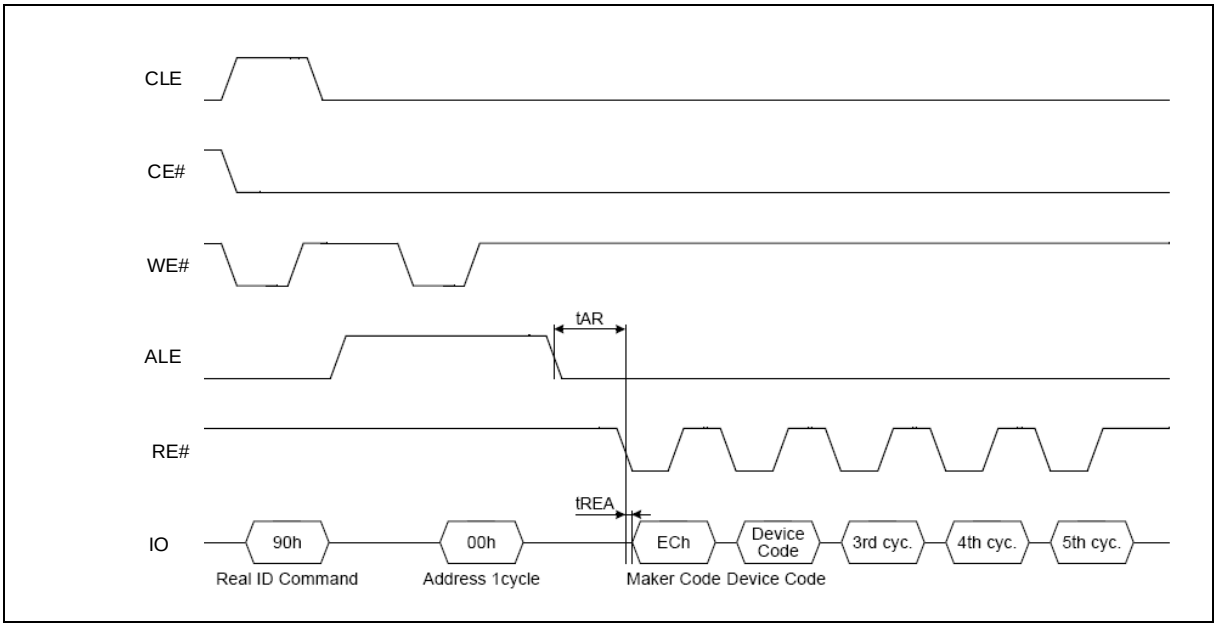


Figure 22 Read ID operation

4. Device Operations

4.1. Page Read

Command 80h + Address 1cycle must be inserted before the Read CMD (00h-30h).

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than 25μs (tR). The system controller can detect the completion of this data transfer (tR) by analyzing the output of R/B# pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

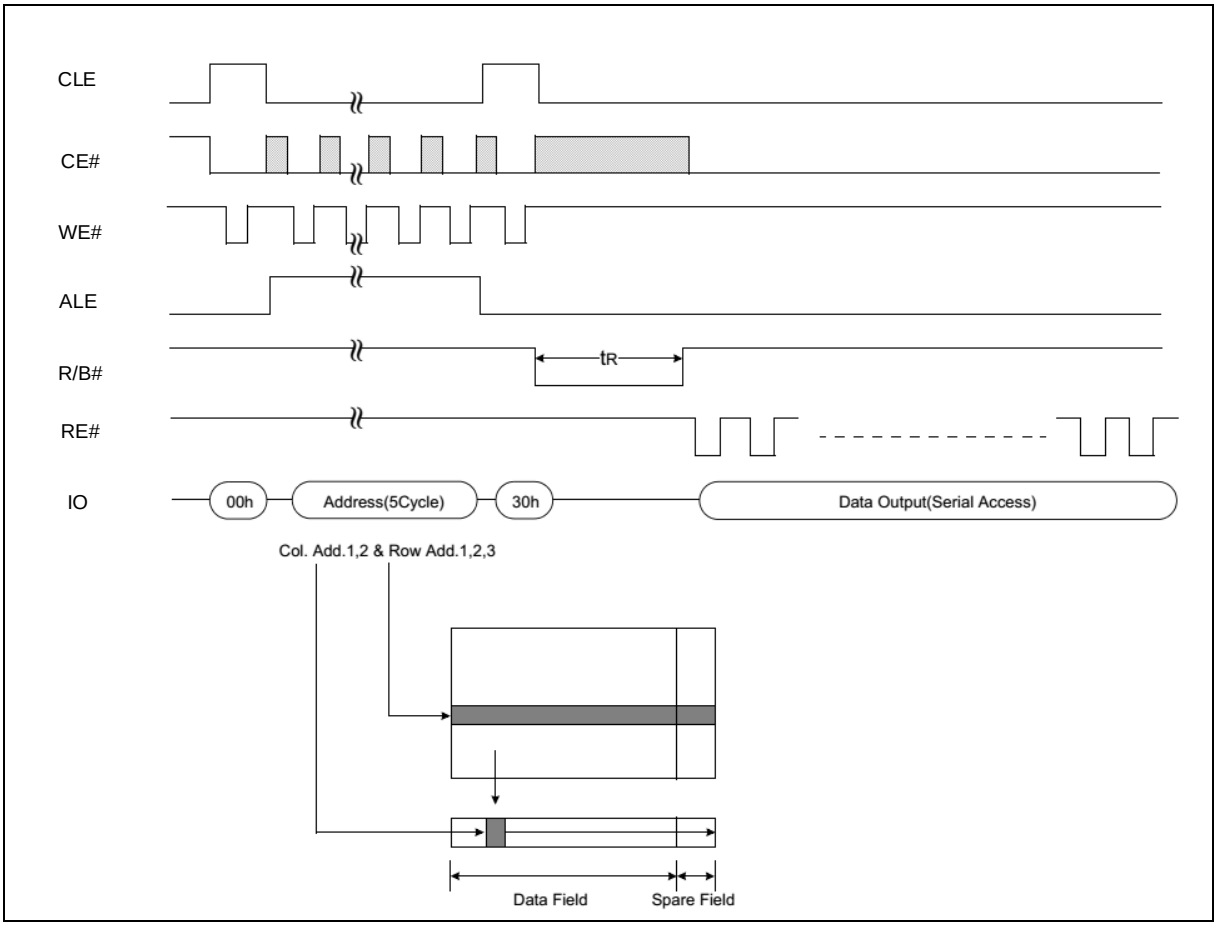


Figure 23 Read Operation

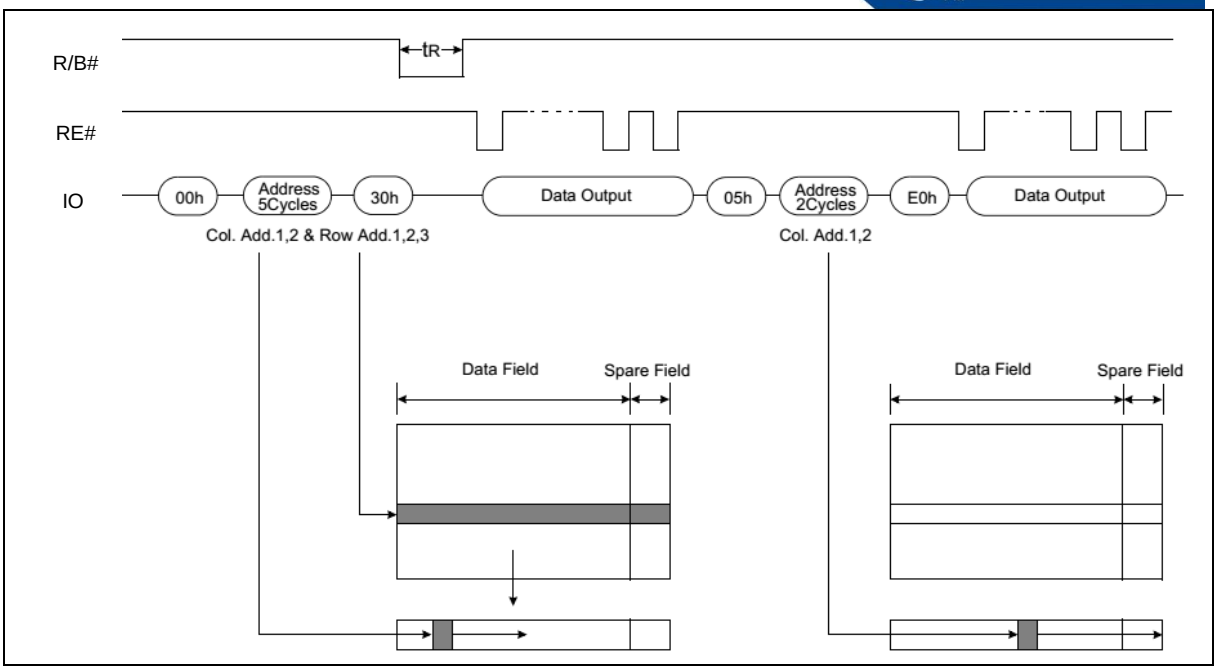


Figure 24 Random Data Output In a Page

4.2. Page Program

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased.

The addressing should be done in sequential order in a block. A page program cycle consist of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

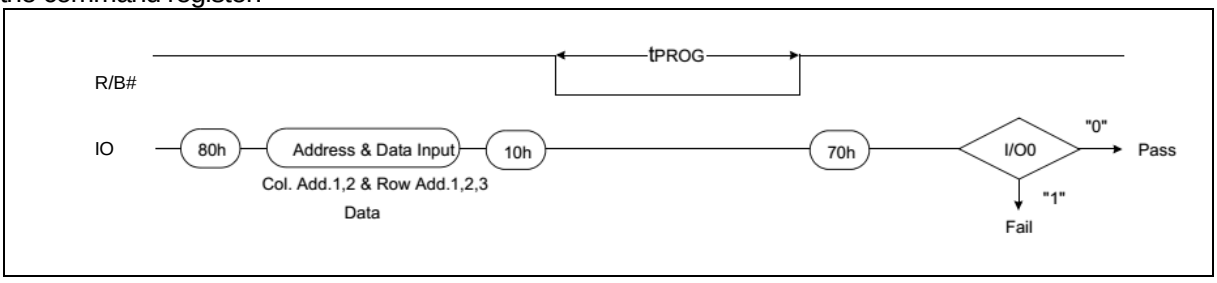


Figure 25 Program & Read Status Operation

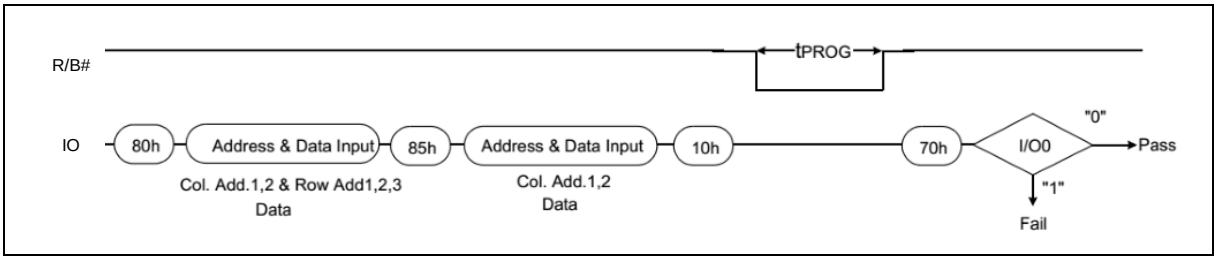


Figure 26 Random Data Input In a Page

4.3. Copy-Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit (I/O0) may be checked. The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h).

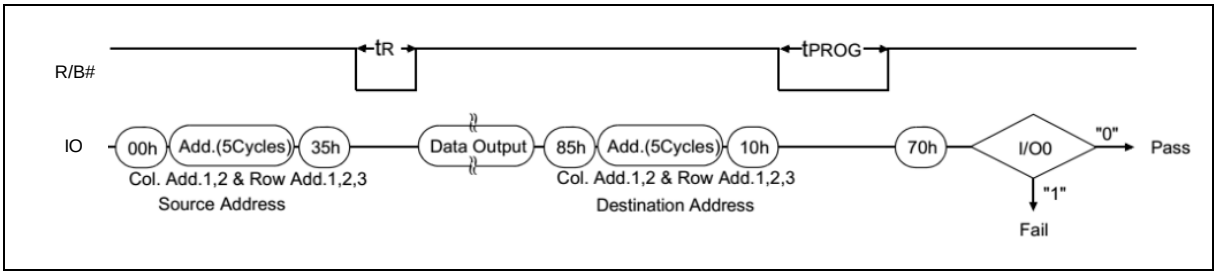


Figure 27 Page Copy-Back Program Operation

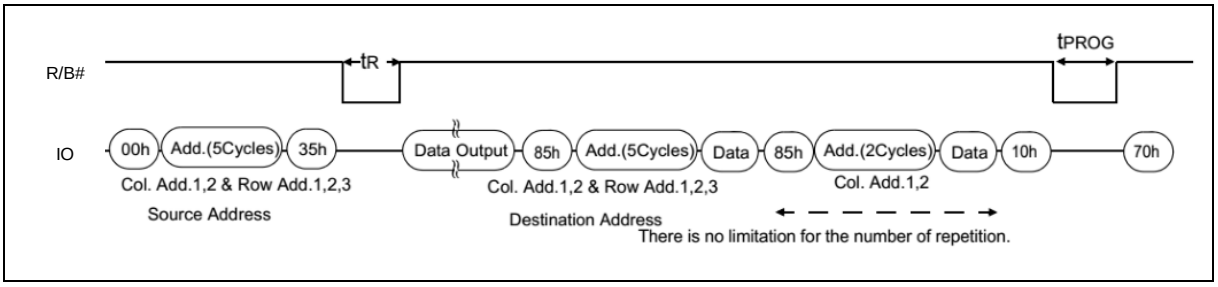


Figure 28 Page Copy-Back Program Operation with random data in

4.4. Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command (60h). Only address A_{18} to A_{29} is valid while A_{12} to A_{17} is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

During the erasing process, only the read status register command and reset command can be accepted, others are ignored.

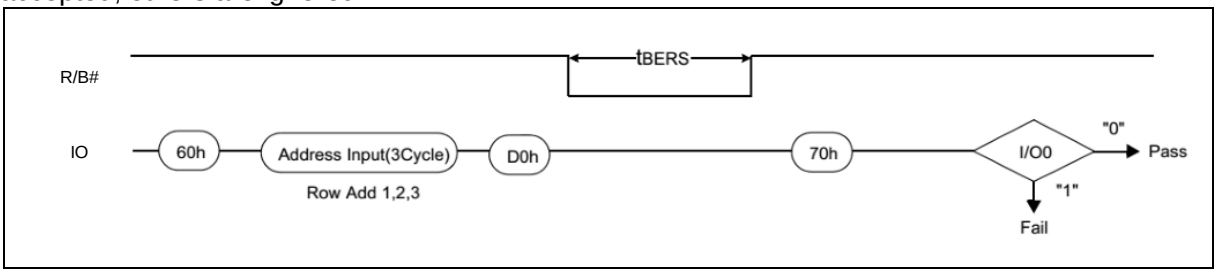


Figure 29 Block Erase Operation

4.5. Unaligned Two-Plane Operation

Two-Plane Read/Program operation is supported in unaligned block addresses, as long as page addresses are same in all planes.

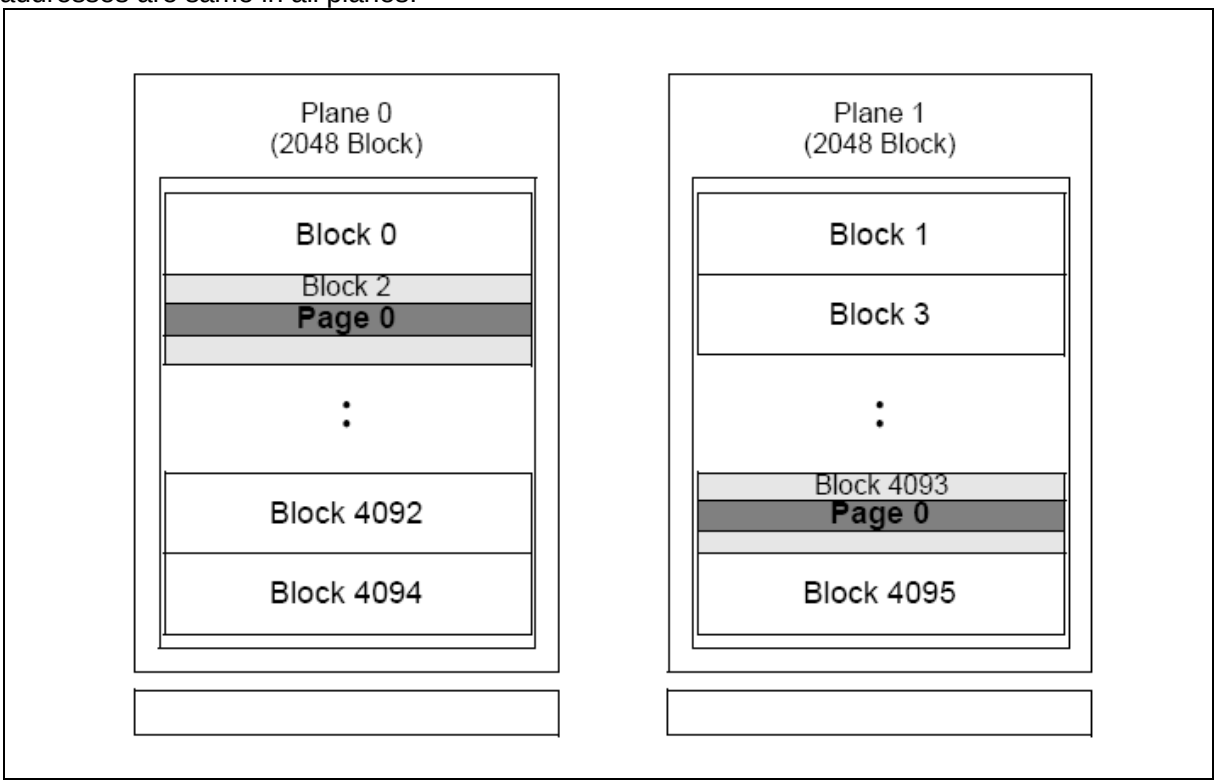


Figure 30 Example of Unaligned Two-Plane Operation

4.6. Two-Plane Page Program Operation

Two-Plane Page Program is an extension of Page Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.

After writing the first set of data up to 2112 byte into the selected page register, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/B# remains in Busy state for a short period of time (t_{DBSY}). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit (I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program (10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Althougth two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails.

Restriction in addressing with Two-Plane Page Program is shown is Figure 31.

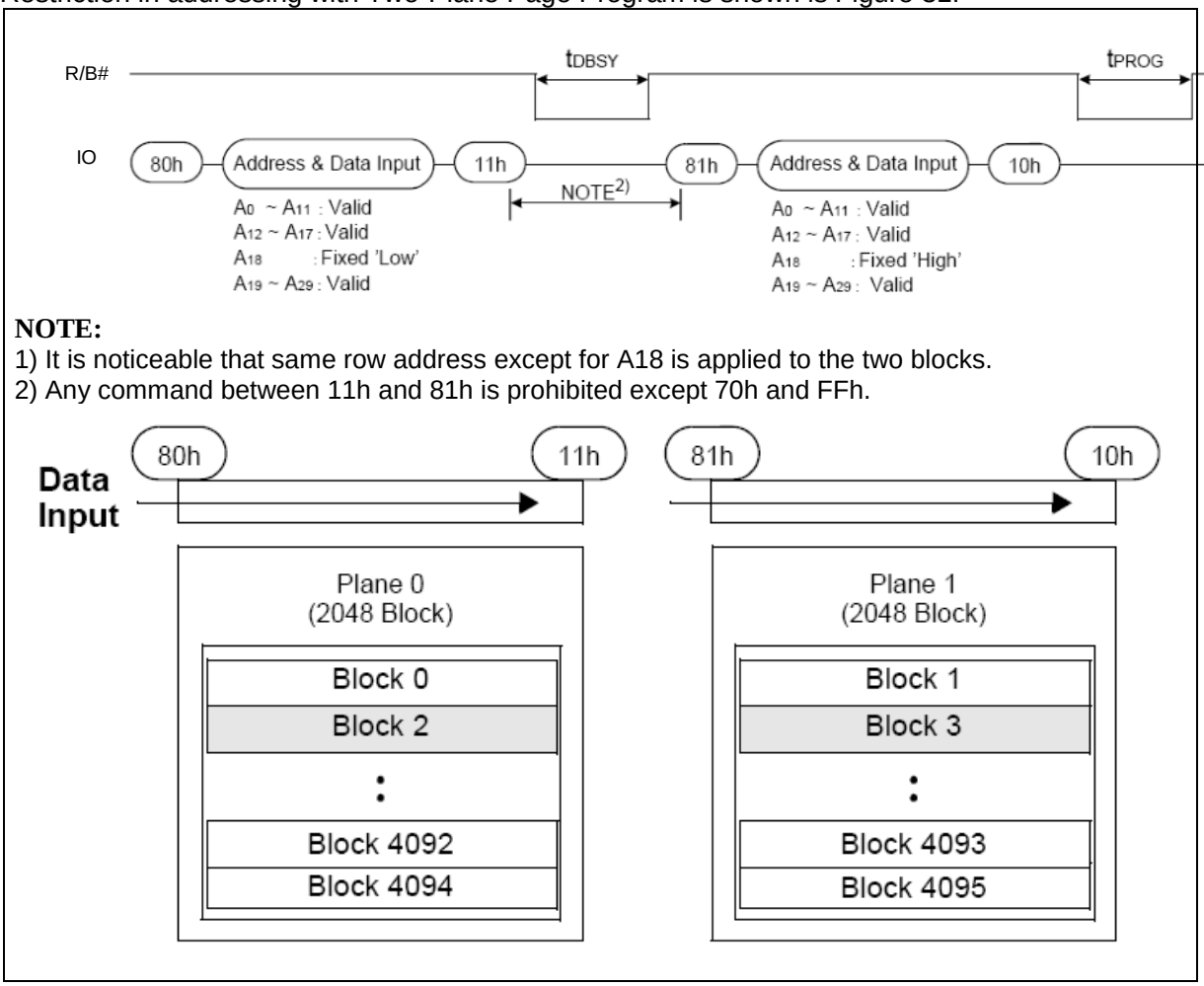
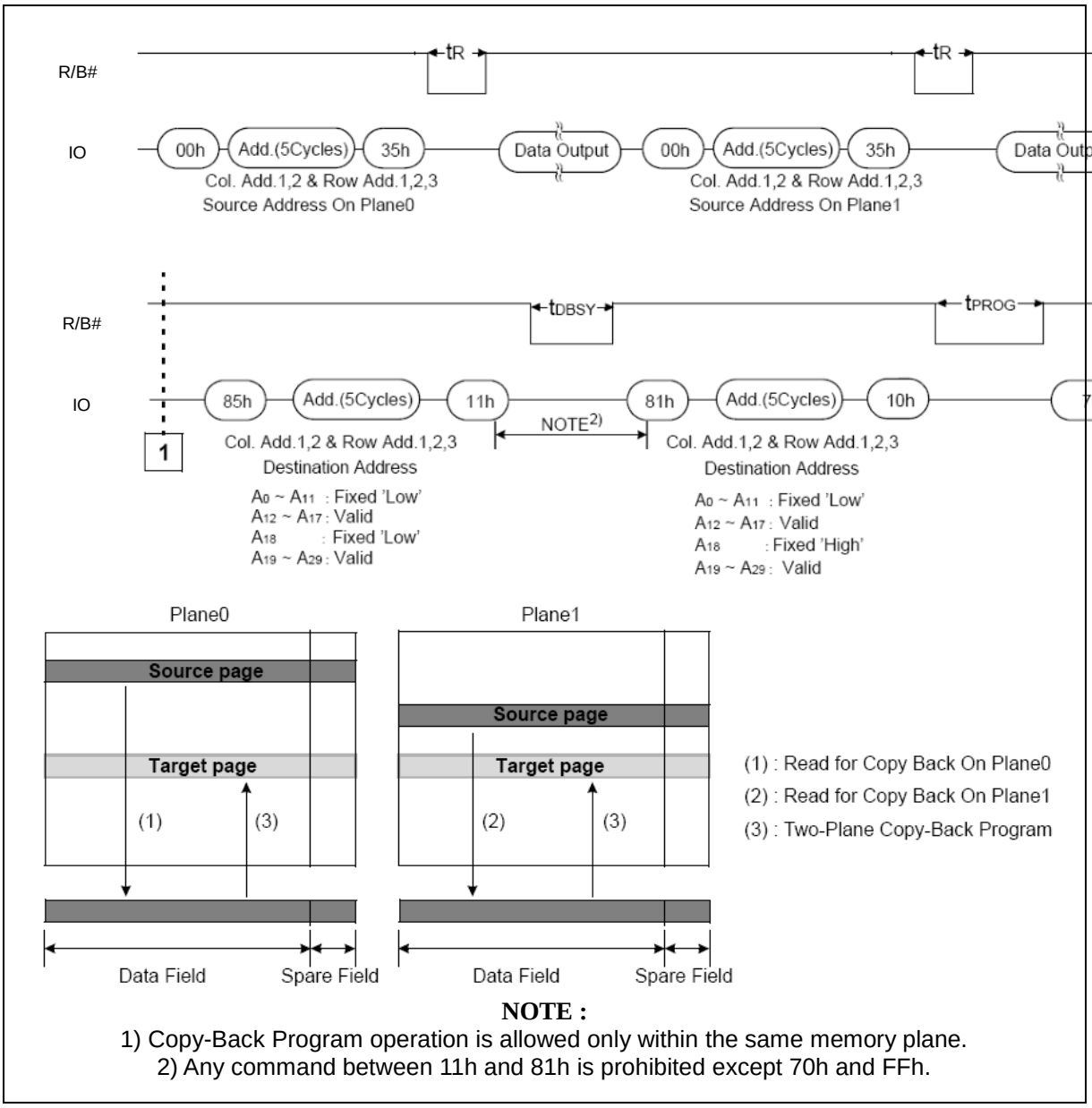


Figure 31 Two-Plane Page Program Sequence

4.7. Two-Plane Copy-Back Program Operation

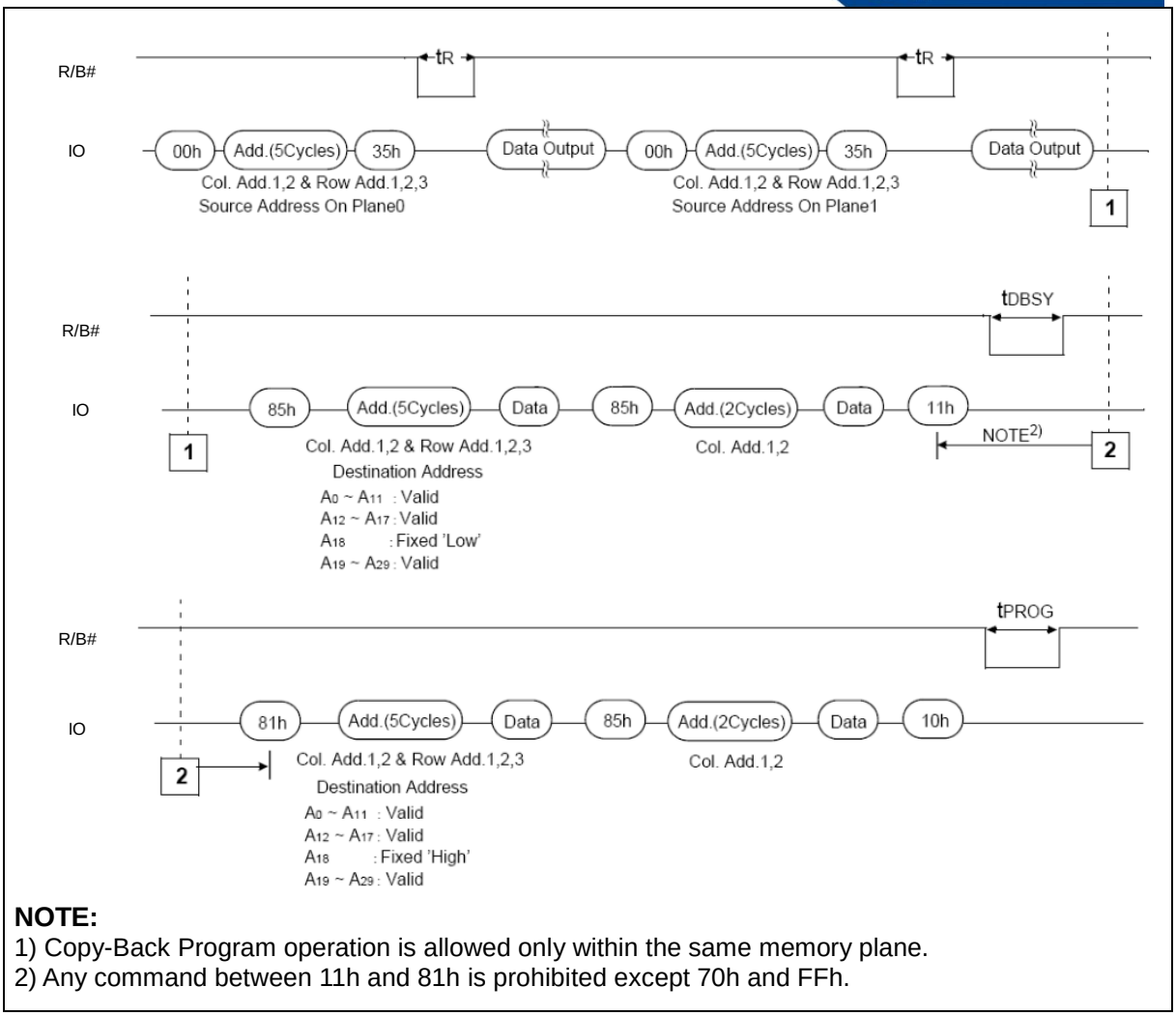
Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages.



NOTE :

1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 32 Two-Plane Copy-Back Program Sequence



NOTE:
1) Copy-Back Program operation is allowed only within the same memory plane.
2) Any command between 11h and 81h is prohibited except 70h and FFh.

Figure 33 Two-Plane Copy-Back Program with Random Data Input Sequence

4.8. Two-Plane Block Erase Operation

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/B pin or Ready/Busy status bit (I/O6).

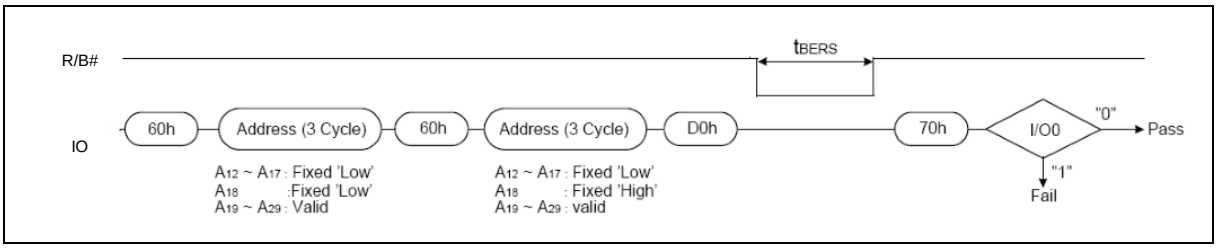


Figure 34 Two-Plane Block Erase Sequence

4.9. Read Status

The device provides a status register that outputs the device status by writing a command code 70h, and then the IO pins output the status at the falling edge of CE# or RE# which occurs last. Even though when multiple flash devices are connecting in system and the R/B# pins are common-wired, the two lines of CE# and RE# may be checked for individual devices status separately. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

Table 2 Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Page Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass: 0 Fail: 1
I/O 1	Not use	Not use	Not use	Not use
I/O 2	Not use	Not use	Not use	Not use
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not use	Not use	Not use	Don't Care
I/O 5	Not use	Not use	Not use	Don't Care
I/O 6	Read/Busy	Read/Busy	Read/Busy	Busy : 0 Ready: 1
I/O 7	Write Protect	Write Protect	Write Protect	Protected: 0 Not Protected: 1

NOTE:

1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

4.10. Read ECC Status

Using the ECC Read Status function, the Error Correction Status can be identified. ECC is performed on the NAND Flash main and spare areas.

The ECC Read Status function also shows the number of errors in a sector as identified from an ECC check during a read operation.

Table 3 ECC Status Bytes

IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Sector Information				ECC Status			

Table 4 ECC Status

IO3 to IO1	ECC Status
0000	No Error
0001	1bit error (Correctable)
0010	2bit error (Correctable)
0011	3bit error (Correctable)
0100	4bit error (Correctable)
Others	Reserved

Table 5 Sector Information

IO7 to IO4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Others	Reserved

4.11. ECC Sector Information

ECC is generated by internal ECC logic during program operation.

During Read operation, the device automatically executes ECC. After read operation is executed, read status command can be issued to identify the read status the read status remains unmodified until other valid commands are executed.

Table 6 2KByte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Table 7 Definition of 528Byte Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1st Sector	0~511	2,048~2,063
2nd Sector	512~1,023	2,064~2,079
3rd Sector	1,024~1,535	2,080~2,095
4th Sector	1,536~2,047	2,096~2,111

NOTE:

1. The Internal ECC manages all data of Main area and Spare area.
2. A sector is the minimum unit for program operation and the number of program per page must not exceed 1.

4.12. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Five read cycles sequentially output the 1st Cycle (ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 35 shows the operation sequence.

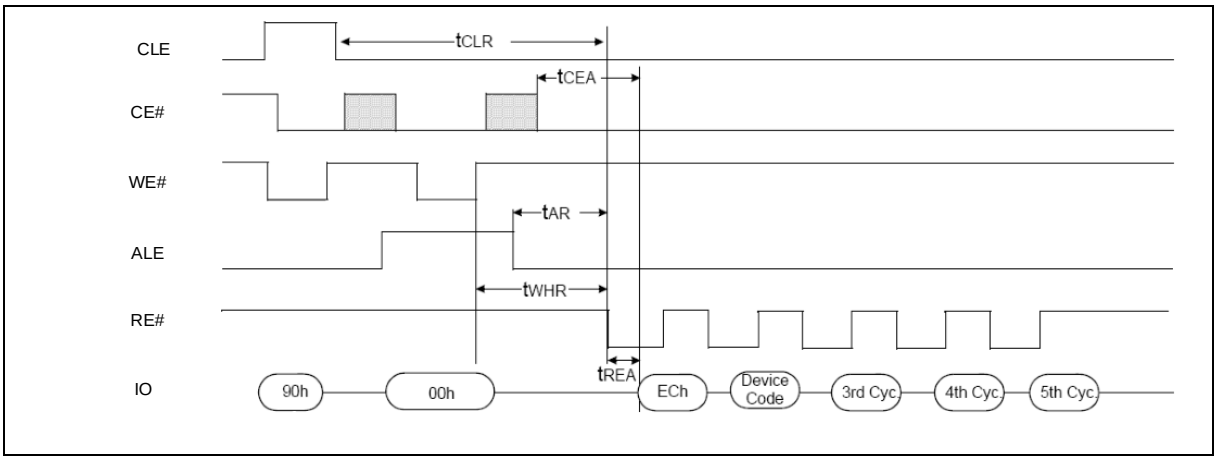


Figure 35 Read ID Operation

Device	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FM29G04C	ECh	DCh	10h	95h	56h

Read ID Definition Table

3rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between multiple chips	Not support		0						
	Support		1						
Cache program	Not Support	0							
	Support	1							

4rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Redundant Area Size (byte/512 Byte)	8						0		
	16						1		
IO Organization	X8		0						
	X16		1						
Serial Access Minimum	50ns/30ns	0				0			
	25ns	1				0			
	Reserved	0				1			
	Reserved	1				1			

5rd ID Data

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size(w/o redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Process	21nm							0	1
	1ynm							1	0
	reserved							0	0
	reserved							1	1
Reserved		0							

4.13. Reset

The reset command FFh resets the read/program/erase operation and clear the status register to be C0h (when WP# is high).

The reset command during the program/erase operation will result in the content of the selected locations (perform programming/erasing) might be partially programmed/erased. If the Flash memory has already been set to reset stage with reset command, the additional new reset command is invalid.

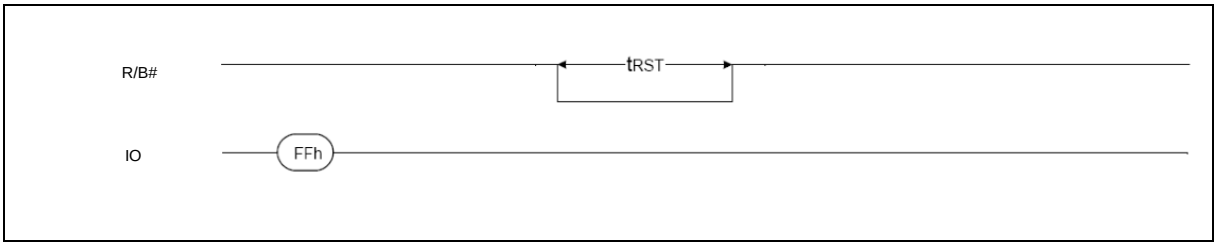


Figure 36 Reset Operation

5. Other Features

5.1. Ready/Busy

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

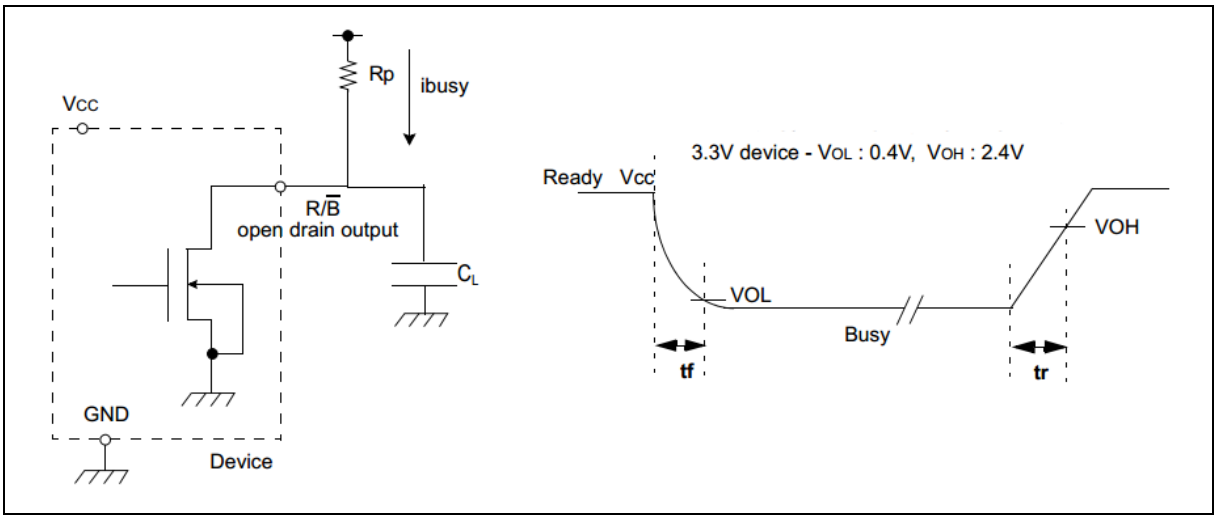


Figure 37 Rp Vs tr,tf & Rp vs ibusy

Rp value Guidance

The rise time of the R/B# signal depends on the combination of R_p and capacitive loading of the R/B# circuit.

It is approximately two times constants (Tc) between the 10% and 90% points on the R/B# waveform.

$T_C = R \times C$

Where $R = R_p$ (Resistance of pull-up resistor), and $C = C_L$(Total capacitive load)

The fall time of the R/B# signal majorly depends on the output impedance of the R/B# signal and the total load capacitance.

$$\text{Rp (Min.)} = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL}$$

NOTE:

1. Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.
2. R_p maximum value depends on the maximum permissible limit of tr.
3. IL is the total sum of the input currents of all devices tied to the R/B# pin.

5.2. Data Protection & Power up sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V. WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. RE# pin is recommended to be kept high during power-up. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in Figure 38. The two step command sequence for program/erase provides additional software protection.

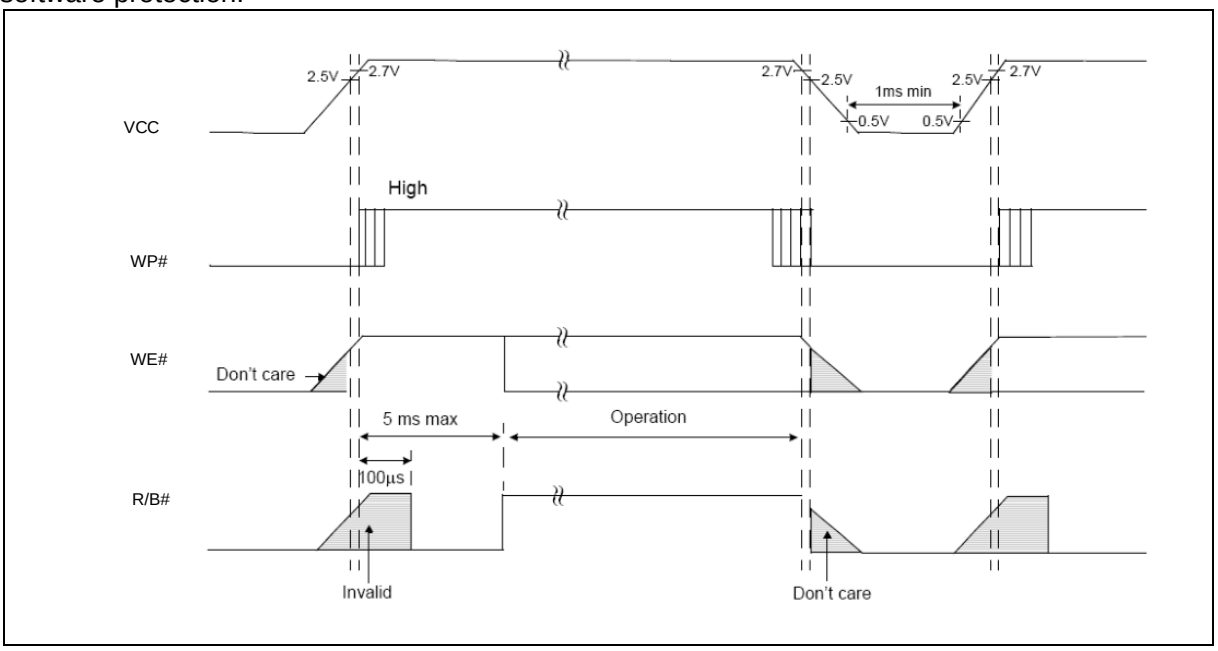


Figure 38 AC Wave forms for Power Transition

NOTE:

1) During the initialization, the device consumes a maximum current of 30mA (ICC1).

2) Once Vcc drops under 2.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

6. NAND Flash Technical Notes

6.1. Initial Invalid Block(s)

The initial invalid blocks are included in the device while it gets shipped called. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. During the time of using the device, the additional invalid blocks might be increasing; therefore, it is recommended to check the invalid block marks and avoid using the invalid blocks. Furthermore, please read out the initial invalid block and the increased invalid block information before any erase operation since it may be cleared by any erase operation.

6.2. Identifying Initial Invalid Block(s)

While the device is shipped, the values of all data bytes of the good blocks are FFh. The initial invalid block(s) status is defined by the 1st byte in the spare area. FM29G04C makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048.

Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart. The erase operation at the invalid block is not recommended.

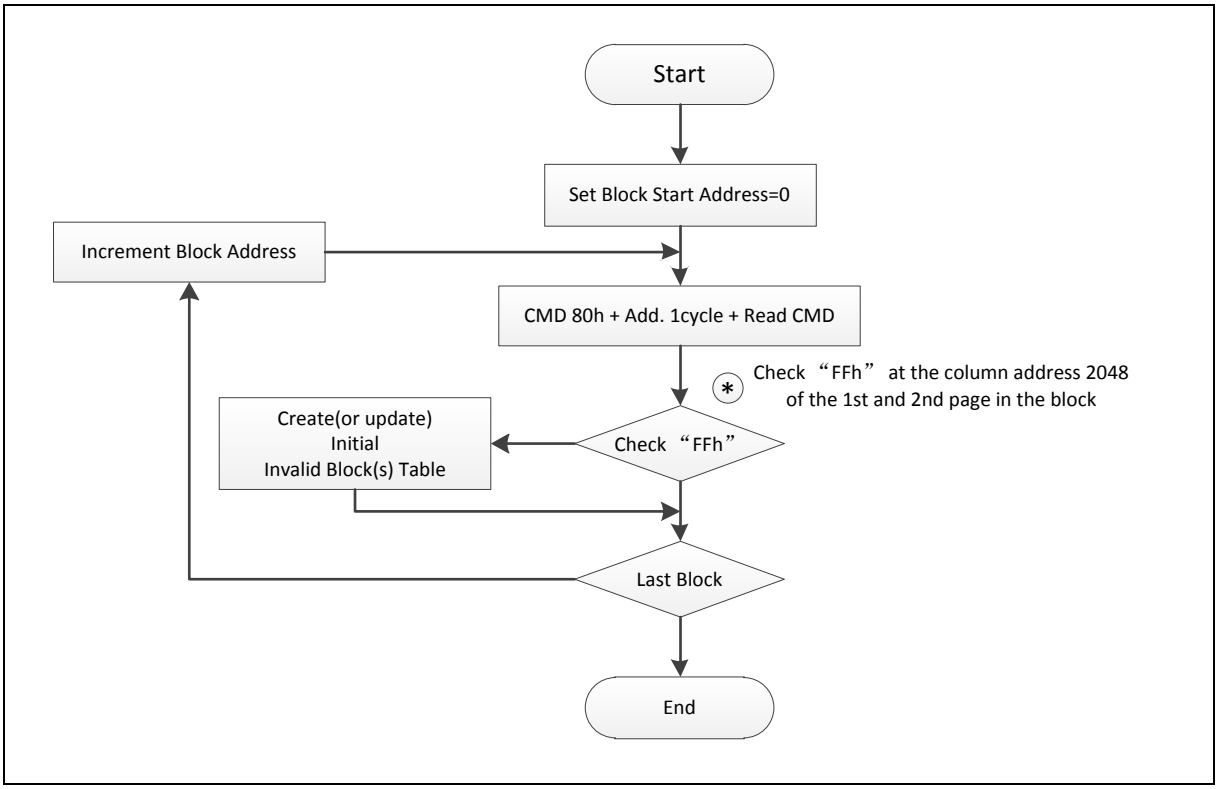


Figure 39 Flow Chart to create initial invalid block table

6.3. Error in write or read operation

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system. Block replacement should be done while status read failure after erase or program. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to error bits be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase-> Block Replacement
	Program Failure	Status Read after Program-> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

Program Flow Chart

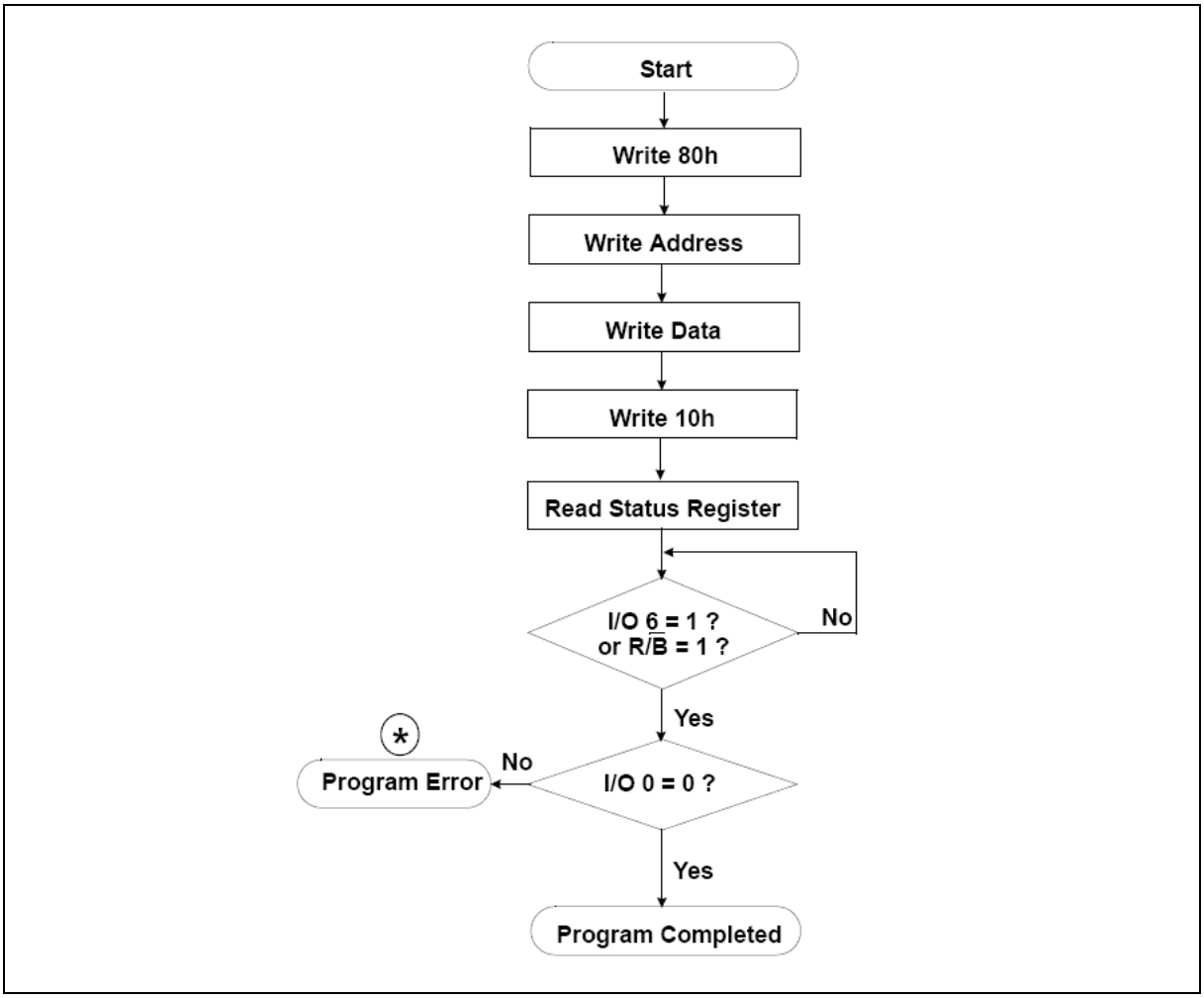
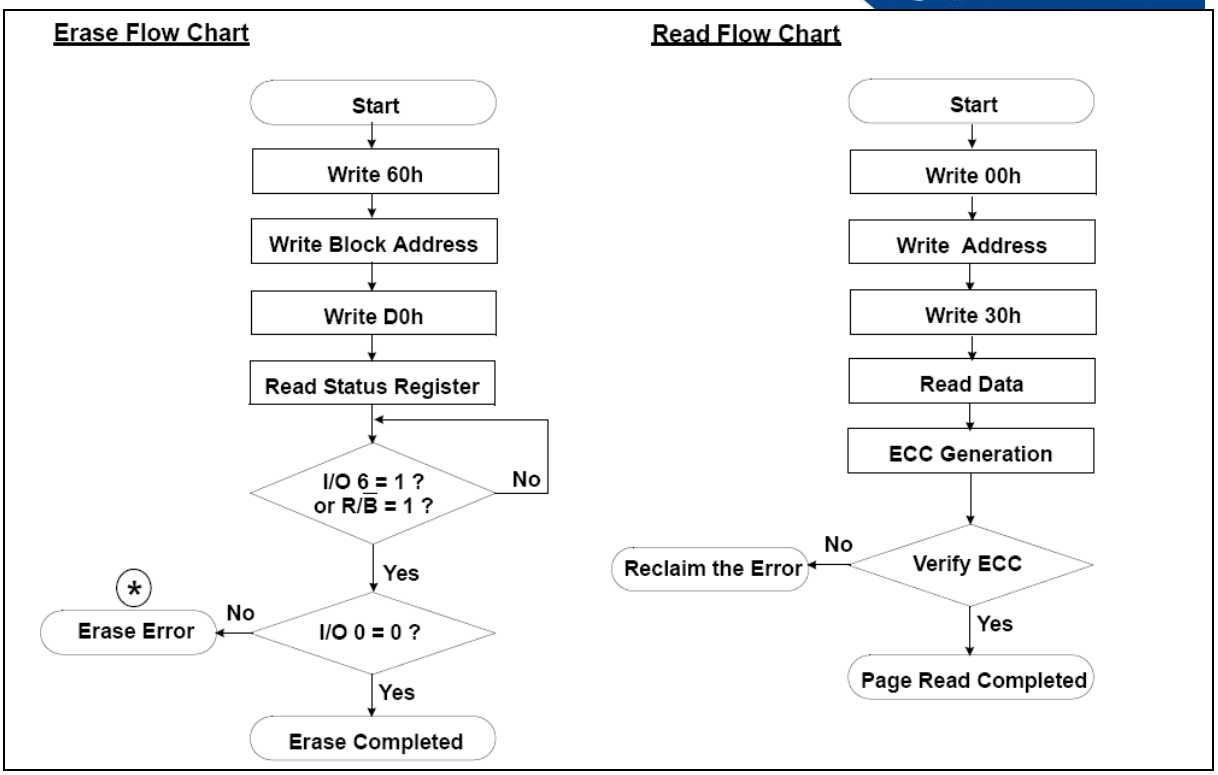


Figure 40 Program Flow Chart

NOTE:
* If program operation results in an error, map out the block including the page in error and copy the target data to another block.



NOTE:
* If erase operation results in an error, map out the failing block and replace it with another block.

Figure 41 Erase and Read Flow Chart

Block Replacement

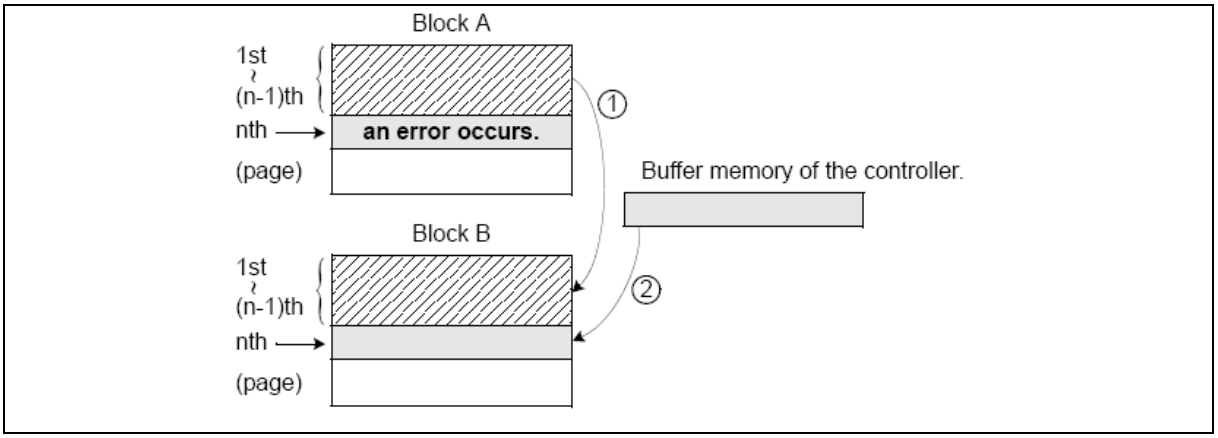


Figure 42 Block Replacement

NOTE:
*Step 1
When an error happens in the nth page of Block A during erase or program operation.
*Step 2
Copy the data in the 1st~(n-1)th page to the same location of another free block (Block B)
*Step 3
Then, copy the nth page data of the Block A in the buffer memory to the nth page of the Block B
*Step 4
Do not erase or program to Block A by creating an invalid block table or other appropriate scheme

6.4. Addressing for Program Operation

Within a block, the page program operation in a block should start from the low address to high address. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.

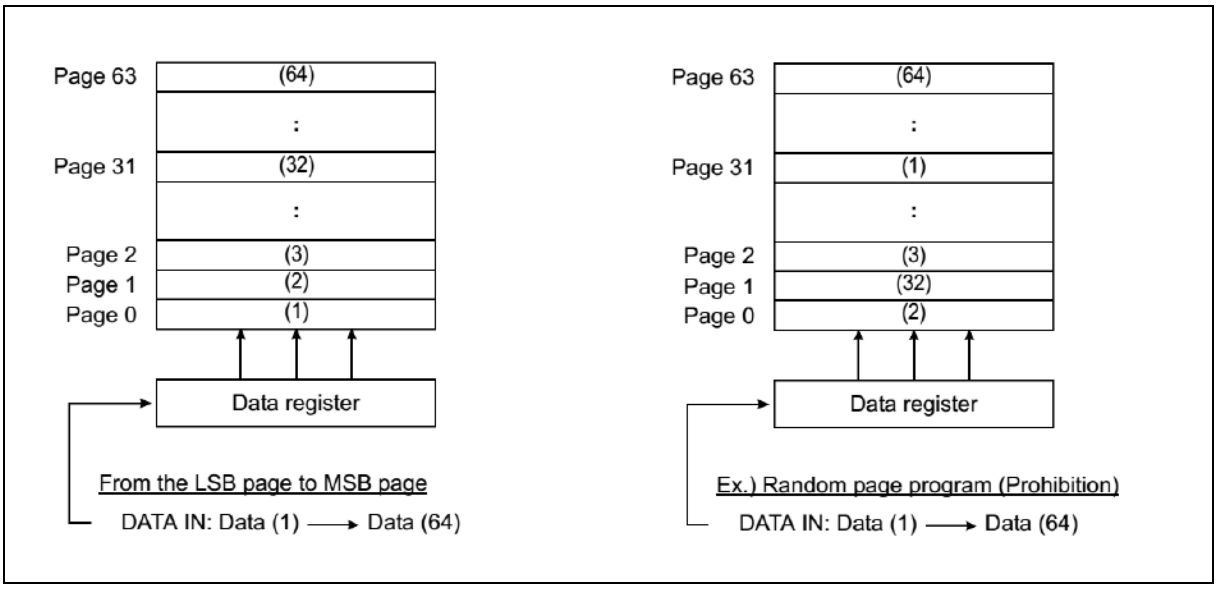
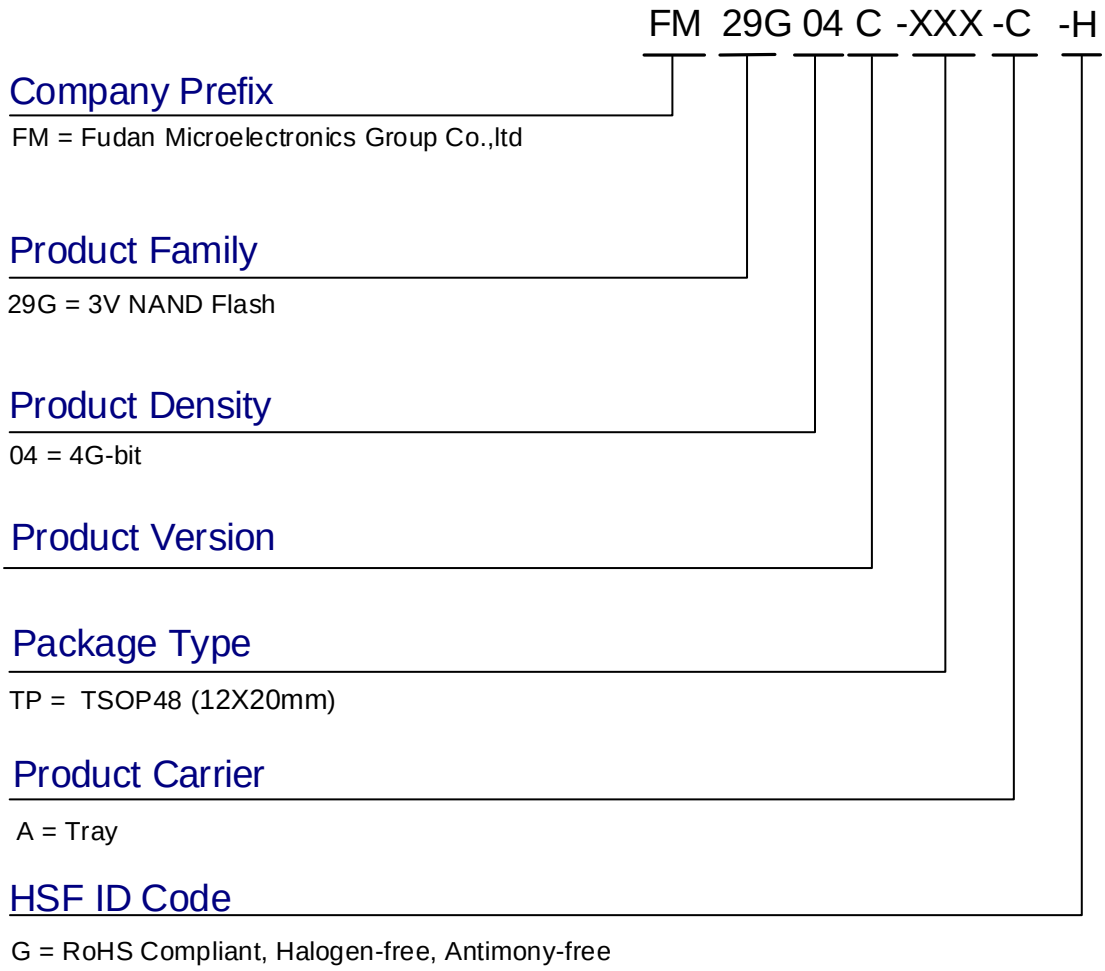


Figure 43 Address for Program Operation

Device	I/O	Data	Address				
			Col.Add1	Col.Add2	Row.Add1	Row.Add2	Row.Add3
FM29G04C	I/O0~I/O7	2112Byte	A0~A7	A8~A11	A12~A19	A20~A27	A28~A29

7. Ordering Information



8. Part Marking Scheme

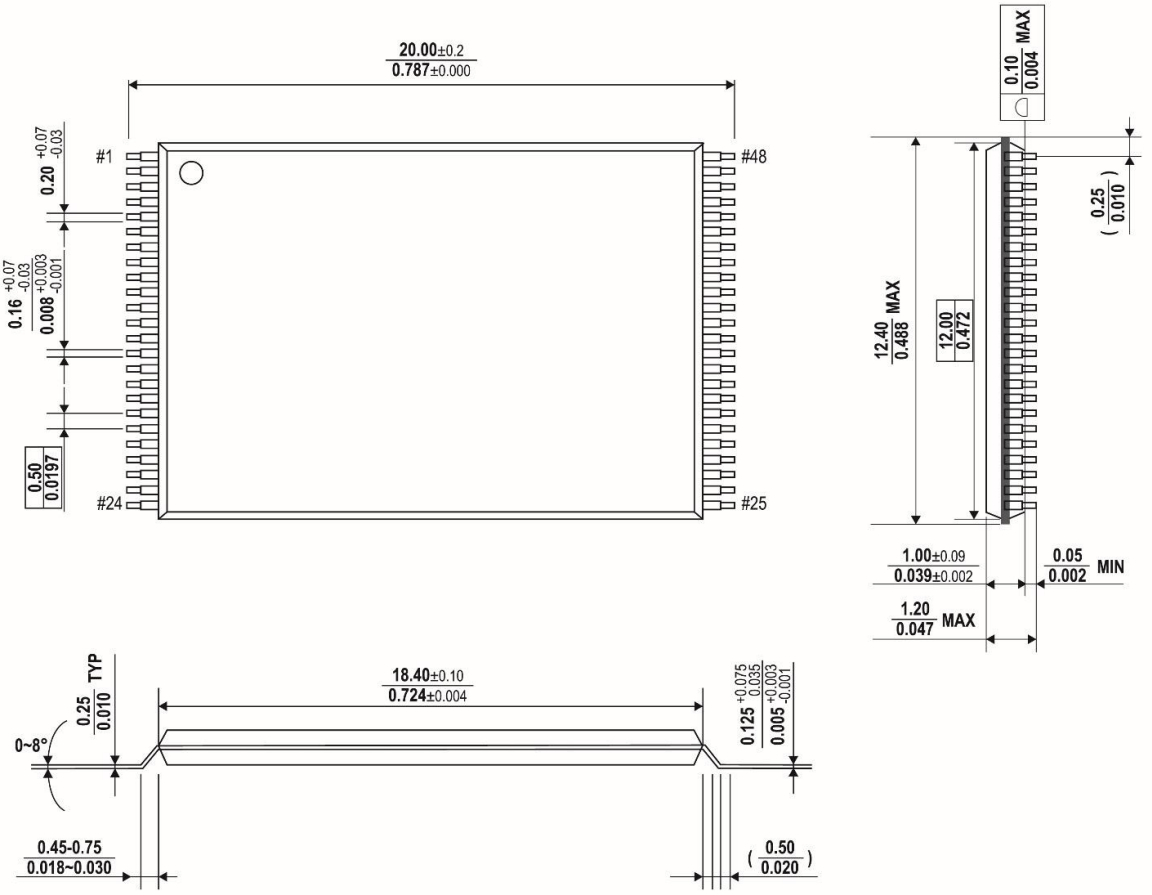
FM29G04C
Product Density

YYWWAALH
HSF ID Code
G = RoHS Compliant, Halogen-free, Antimony-free
Package Lot Number (just with 0~9, A~Z)
Assembly's Code
Work week during which the product was molded (eg..week 12)
The last two digits of the year in which the product was sealed/molded

XXXXXXXX
Wafer Lot Number (the length is not fixed)

9. Packaging Information

TSOP48 (12X20mm)



10. Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
Preliminary	Jun. 2018	47		Initial document Release.

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